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## 易翔 Yi Xiang



### 基本信息

职称：微电子学院教授、博导、硕导

Title: Professor, Doctoral &  
Graduate Supervisor, School of Microelectronics

联系方式: yixiang@scut.edu.cn

## 招生专业



博士

【学术型】电子科学与技术（微电子学与固体电子学）

【专业型】电子信息（电子工程）



硕士

【学术型】电子科学与技术（微电子学与固体电子学）

【专业型】电子信息（集成电路工程）

## 个人简介

易翔，博士毕业于南洋理工大学，先后于南洋理工大学和麻省理工学院开展博士后研究工作。主要研究方向为：射频、毫米波和太赫兹频率综合器、通信和雷达收发机集成电路设计。作为共同主持人或项目负责人领导了约1670万人民币的项目，其中作为共同主持人的项目为960万人民币。发表包括JSSC和ISSCC在内的论文50余篇，出版英文学术专著2部，申请专利10余项。为电气和电子工程师协会（IEEE）高级会员，担任IEEE JSSC、TMTT、TCAS-I等多个国际期刊审稿人及ISCAS评审委员会委员，获IEEE ISSCC丝绸之路奖和ISSCC STGA奖。

Dr. Xiang Yi got his Ph.D. degree from Nanyang Technological University. He worked as the postdoc in Nanyang Technological University and Massachusetts Institute of Technology. His main research fields are RF, millimeter wave and terahertz frequency synthesizer, communication and radar transceivers IC design. He co-PI or led about 16.7 million RMB projects, including 9.6 million RMB co-PI projects. He

has published more than 50 papers including JSSC and ISSCC, published two English academic books, and applied for more than 10 patents. Dr. Yi is a Senior Member of the Institute of Electrical and Electronic Engineers (IEEE), the reviewer of IEEE JSSC, TMTT, TCAS-I and other international journals, and ISCAS Review Committee Member. He won IEEE ISSCC Silkroad award and ISSCC STGA award.

## 教育经历

2002.09 - 2006.06	华中科技大学	学士
2006.09 - 2009.06	华南理工大学	硕士
2009.08 - 2014.07	南洋理工大学	博士
2014.07 - 2017.07	南洋理工大学	博士后
2017.07 - 2020.09	麻省理工学院	博士后

## 工作经历

2021.01至今	华南理工大学	特聘教授
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## 研究方向

射频、毫米波和太赫兹频率综合器、通信和雷达收发机集成电路设计。

## 授课课程

模拟集成电路设计

## 学术任职

IEEE高级会员

IEEE JSSC、TMTT、TCAS-I等多个国际期刊审稿人

ISCAS评审委员会委员

## 科研项目

新加坡教育部Tier 2项目“先高分辨率超低功耗集成成像器”，2013.7-2016.06 负责人

新加坡教育部Tier 1项目“先进CMOS工艺的单片太赫兹无源元件：从基础研究到集成电路应用”，2016.11-2017.07 负责人

新加坡横向项目（格罗方德）“基于氮化镓的DC-DC转换器电路设计”，2016.06-2017.07 负责人

新加坡横向项目（华为）“下一代无线局域网802.11ax的收发机芯片研发”，2014.07-2017.07 共同主持

新加坡横向项目（台达电子）“用于内容驱动学习媒体传输的无线异构网络收发器芯片”，2016.07-2017.07 共同主持

美国横向项目（台积电）“芯片级太赫兹三维成像雷达”，2017.07-2020.09 负责人

美国横向项目（林肯实验室）“全双工收发机”，2018.10-2020.09 负责人

美国横向项目（德州仪器）“芯片级分子钟”，2017.07-2020.09 核心成员

## 代表性科研成果

- [1] X. Yi, J. Wang, C. Wang, K. E. Kolodziej and R. Han, “Realization of In-Band Full-Duplex Operation at 300 K and 4.2 K Using Bilateral Single-Sideband Frequency Conversion,” *IEEE J. Solid-State Circuits*, accepted.
- [2] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, A 220-to-320-GHz FMCW Radar in 65-nm CMOS Using A Frequency-Comb Architecture, *IEEE J. Solid-State Circuits*, vol. 65, no. 2, pp.327–339, Feb. 2021.
- [3] K. Yang, X. Yi, C. C. Boon, Z. Liang, G. Feng, C. Li, B. Liu, A Parallel Sliding-IF Receiver Front-End with Sub-2 dB Noise Figure for 5-6 GHz WLAN Carrier Aggregation, *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp.392–403, Feb. 2021.
- [4] C. Wang, X. Yi, M. Kim, Q. Yang and R. Han, A Terahertz Molecular Clock on CMOS Using High-Harmonic-Order Interrogation of Rotational Transition for Medium/Long-Term Stability Enhancement, *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp.566–580, Feb. 2021.
- [5] X. Yi, J. Wang, C. Wang, K. E. Kolodziej and R. Han, “A 3.4–4.6-GHz In-Band Full-Duplex Front-End in CMOS Using A Bi-Directional Frequency Converter,” in *RFIC Symp. Dig. Papers*, Jun. 2020, pp. 47–50.
- [6] X. Yi, C. Wang, M. Lu, J. Wang, J. Grajal and R. Han, A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth, in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 90–91.
- [7] C. Wang, X. Yi, M. Kim and R. Han, Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot Array Couplers, in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 448–449.
- [8] X. Yi, Z. Liang, C.C. Boon, G. Feng, F. Meng, and K. Yang, “An Inverted Ring Oscillator Noise-Shaping Time-to-Digital Converter with In-band Noise Reduction and Coherent Noise Cancellation, *IEEE Trans. on Circuits and Systems-I: Regular Papers*, vol. 67, no. 2, pp. 686–698, Feb. 2020.
- [9] B. Liu, \*X. Yi, K. Yang, Z. Liang, G. Feng, P. Choi, C. C. Boon, and C. Li, “A Carrier Aggregation Transmitter Front-End for 5-GHz WLAN 802.11ax Application in 40nm CMOS,” *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 1, pp. 264–276, Jan. 2020.
- [10] C. Li, \*X. Yi, C. C. Boon, and K. Yang, “A 34 dB Dynamic Range 0.7 mW Compact Switched-Capacitor Power Detector in 65 nm CMOS,” *IEEE Trans. on Power Electronics*, vol. 34, no. 10, pp. 9365–9368, Oct. 2019.
- [11] X. Yi, Z. Liang, G. Feng, F. Meng, C. Wang, C. Li, K. Yang, B. Liu, and C. C. Boon, “A 93.4-to-104.8GHz 57mW fractional- $N$  cascaded PLL with true in-phase injection-coupled QVCO in 65nm CMOS Technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 6, pp.2370–2381, Jun. 2019.
- [12] C. Wang, X. Yi, J. Mawdsley, M. Kim, Z. Wang, R. Han, “An on-chip fully-electronic molecular clock based on sub-terahertz rotational spectroscopy,” *Nature Electronics*, Vol. 1, No. 7, Jul. 2018.
- [13] X. Yi, K. Yang, Z. Liang, B. Liu, K. Devrishi, C. C. Boon, C. Li, G. Feng, D. Regev, S. Shilo, F. Meng, H. Liu, J. Sun, G. Hu, and Y. Miao, “A 65nm CMOS carrier-aggregation transceiver for IEEE 802.11 WLAN applications,” in *RFIC Symp. Dig. Papers*, May. 2016, pp.67–70.
- [14] X. Yi, Z. Liang, G. Feng, C. C. Boon, and F. Meng, “A 93.4-to-104.8 GHz 57 mW fractional- $N$  cascaded sub-sampling PLL with true in-phase injection-coupled QVCO in 65 nm CMOS,” in *RFIC Symp. Dig. Papers*, May 2016, pp.122–125.

- [15] X. Yi, C. C. Boon, H. Liu, J. Lin, and W. M. Lim, "A 57.9-to-68.3 GHz 24.6 mW frequency synthesizer with in-phase injection-coupled QVCO in 65 nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp.347–359, Feb. 2014.
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- [17] X. Yi, C. C. Boon, H. Liu, J. Lin, J. C. Ong, and W. M. Lim, "A 57.9-to-68.3GHz 24.6mW frequency synthesizer with in-phase injection-coupled QVCO in 65nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 354–355.
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### 本科生培养

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#### 师资概况

(</microelectronics/szgj/list.htm>)

#### 博导

(</microelectronics/bd/list.htm>)

#### 硕导

(</microelectronics/sd/list.htm>)

#### 实验人员

(</microelectronics/syry/list.htm>)

兼职教授 / 客座  
教授 / 兼职教师

### 联系我们

地址：广州市天河区五山路381号/广州市番禺区兴业大道东777号广州国际校区

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