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Robust Signaling Techniques for Through Silicon Via Bundles

Authors

Krishna Chaitanya Chillara, *University of Massachusetts Amherst* Follow

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Abstract

3D circuit integration is becoming increasingly important as one of the remaining techniques for staying on Moore's law trajectory. 3D Integrated Circuits (ICs) can be realized using the Through Silicon Via (TSV) approach. In order to extract the full benefits of 3D and for better yield, it has been suggested that the TSVs should be arranged as bundles rather than parallel TSVs. TSVs are required to route the signals through different dies in a multi-tier 3D IC. TSVs are excellent but scarce electrical conductors. Hence, it is important to utilize these resources very efficiently.

In high performance 3D ICs, signaling techniques play a crucial role in determining the overall performance of the system. In this work, 3x3 and 4x4 TSV bundles are considered. Electrical parasitics of TSV bundles are extracted using Ansoft Q3D Extractor. Various techniques for signaling over TSV bundles are analyzed in this work. Performance, energy and robustness are the crucial aspects to be considered for analyzing a signaling technique. For performance analysis, maximum data rate for each of the signaling techniques is obtained and the dominant factors that determine these values are identified. 3D integration is fairly a new field and does not have common standards. Different research groups (both academic and industry) across the globe have different manufacturing technologies to suit their needs. In this work, we obtain the electrical parasitics of TSV bundles for different TSV radii ranging from 1mm to 15mm. The TSV radius for most of the 3D integration technologies falls within this range. Maximum data rates are determined for different TSV radii ranging from 1mm to 15mm. This study across different TSV radii helps in choosing a better signaling technique for a particular TSV radius depending on the design goals. Energy/bit for each of the signaling techniques is obtained for a common data rate of 10Gbps Pseudo Random Bit Sequence (PRBS) input. For robustness analysis, the impact of process, voltage and temperature variations between driver and receiver circuits is analyzed. Ansoft Q3D extractor, NCSU 45nm PDK and HSPICE simulation tool are used.

From the simulation results, it is observed that a differential technique is beneficial for smaller radii in terms of maximum data rate that can be obtained. For a radius above 7mm, single ended current mode signaling gives a better data rate. Low swing single ended signaling techniques consume less energy but suffer slightly more due to process variations compared to full swing voltage mode signaling. In terms of robustness to supply noise, differential signaling is more robust compared to single ended techniques. An increase in the temperature reduces the data rates of both single ended and differential signaling techniques. Hence, depending on the TSV radius of target technology and process and environment variations, an optimum signaling technique can be chosen.

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