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Critical Area Driven Dummy Fill Insertion to Improve Manufacturing Yield

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Abstract
Non-planar surface may cause incorrect transfer of patterns during lithography. In today's IC manufacturing, chemical mechanical polishing (CMP) is used for topographical planarization. Since polish rates for metals and oxides are different, dummy metal fills in layout is used to minimize post-CMP thickness variability. Traditional metal fill solutions focus on satisfying density target determined by layout density analysis techniques. These solutions may potentially reduce yield by increasing probability of failure (POF) due to particulate defects and also impact design performance. Layout design solutions that minimize POF and also improve surface planarity via dummy fill insertions have competing requirements for line spacing. In this thesis, I present a formulation to balance these competing goals and provide a comparative study of greedy (or fixed spacing), variable spacing and LP formulation based fill insertions based on scalability and quality of solution. I extend the variable spacing fill to allow non-preferred direction routing of fill patterns

in order to further improve the CA. Traditional fill solutions impact design performance due to increase coupling capacitance on signal nets. I present a fill insertion algorithm that minimizes this increase in coupling capacitance due to fill. Finally, I extend the critical area based solution to include SRAF insertion in order to account for optical diffraction in lithography.

Thus the proposed solution addresses both lithography and particulate related defects and minimizes the fill impact on design performance at the same time. Experimental results based on layout of ISCAS 85 benchmark circuits show that the variable spacing and the LP formulation based fill insertion techniques result in substantially reduced critical area while satisfying the layout density and uniformity criteria. The coupling capacitance minimization fill solution reduces the fill impact on coupling capacitance while at the same time minimizing the critical area.

Advisor(s) or Committee Chair
Kundu, Sandip

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