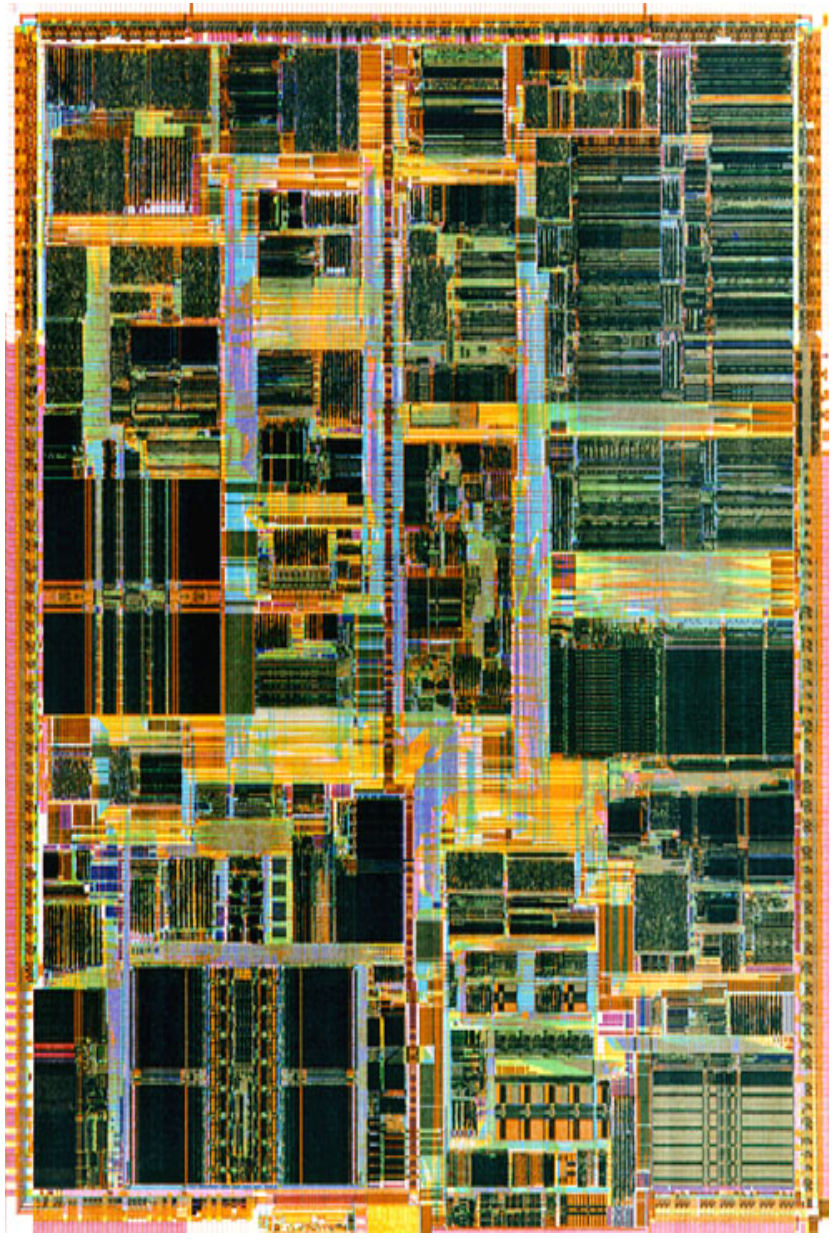


半导体集成电路

学校：西安理工大学

院系：自动化学院电子工程系

专业：电子、微电

时间：秋季学期

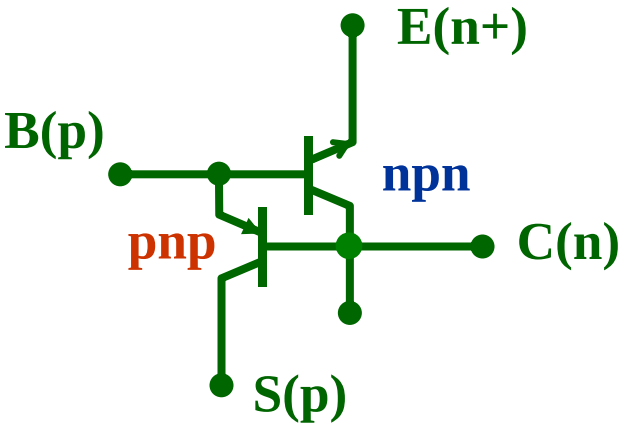
上节课内容要点

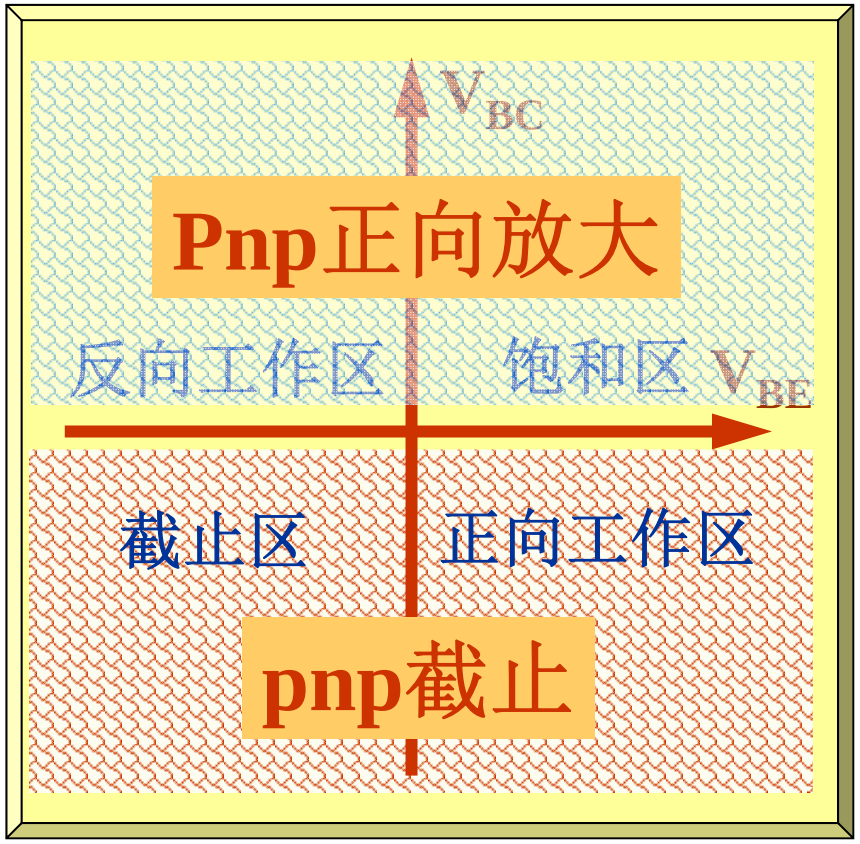
1. 两结三层双极晶体管的EM模型

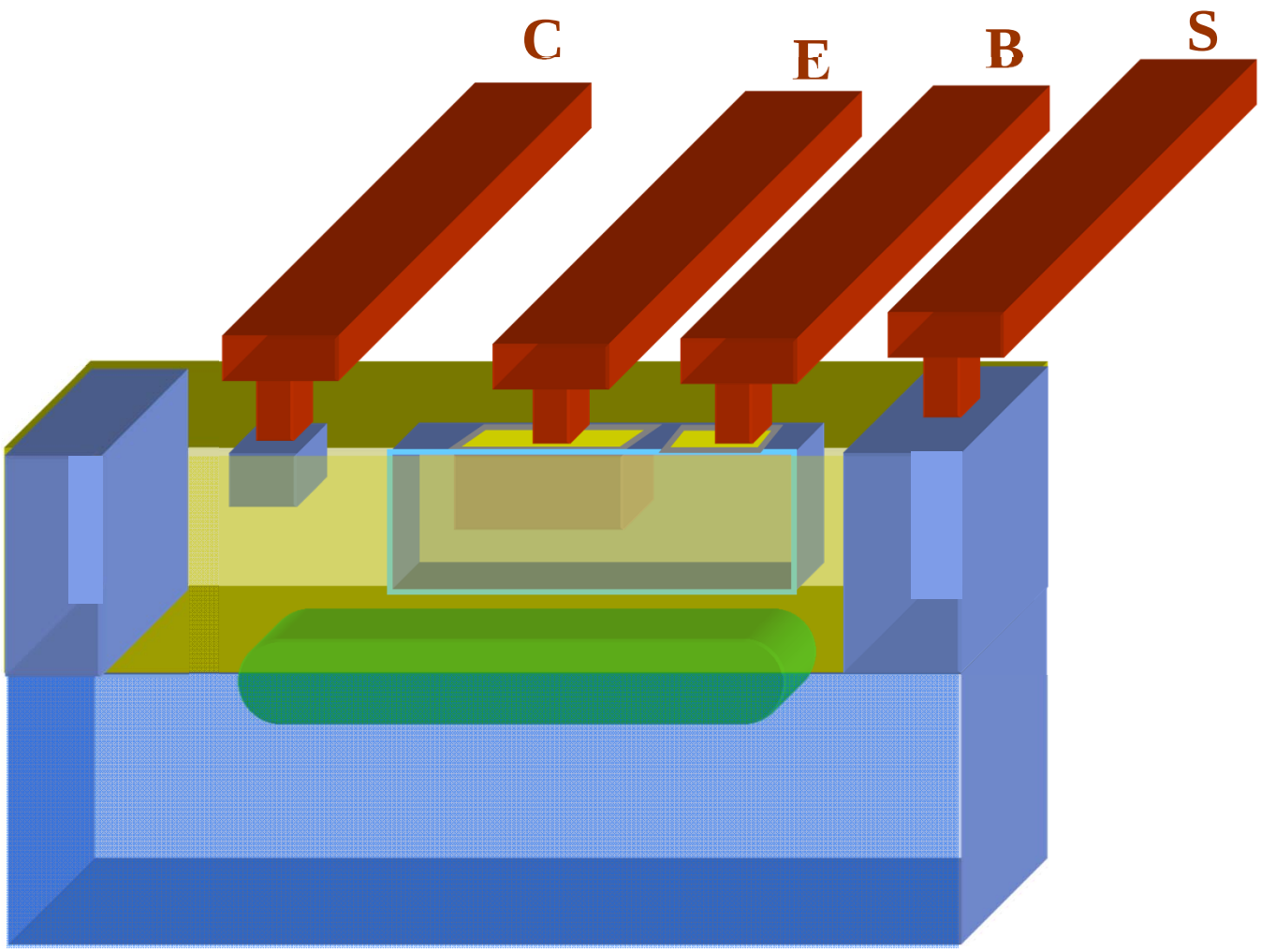
2. 三结四层双极晶体管的EM模型

◆基本要求

- 双极晶体管的四种工作状态



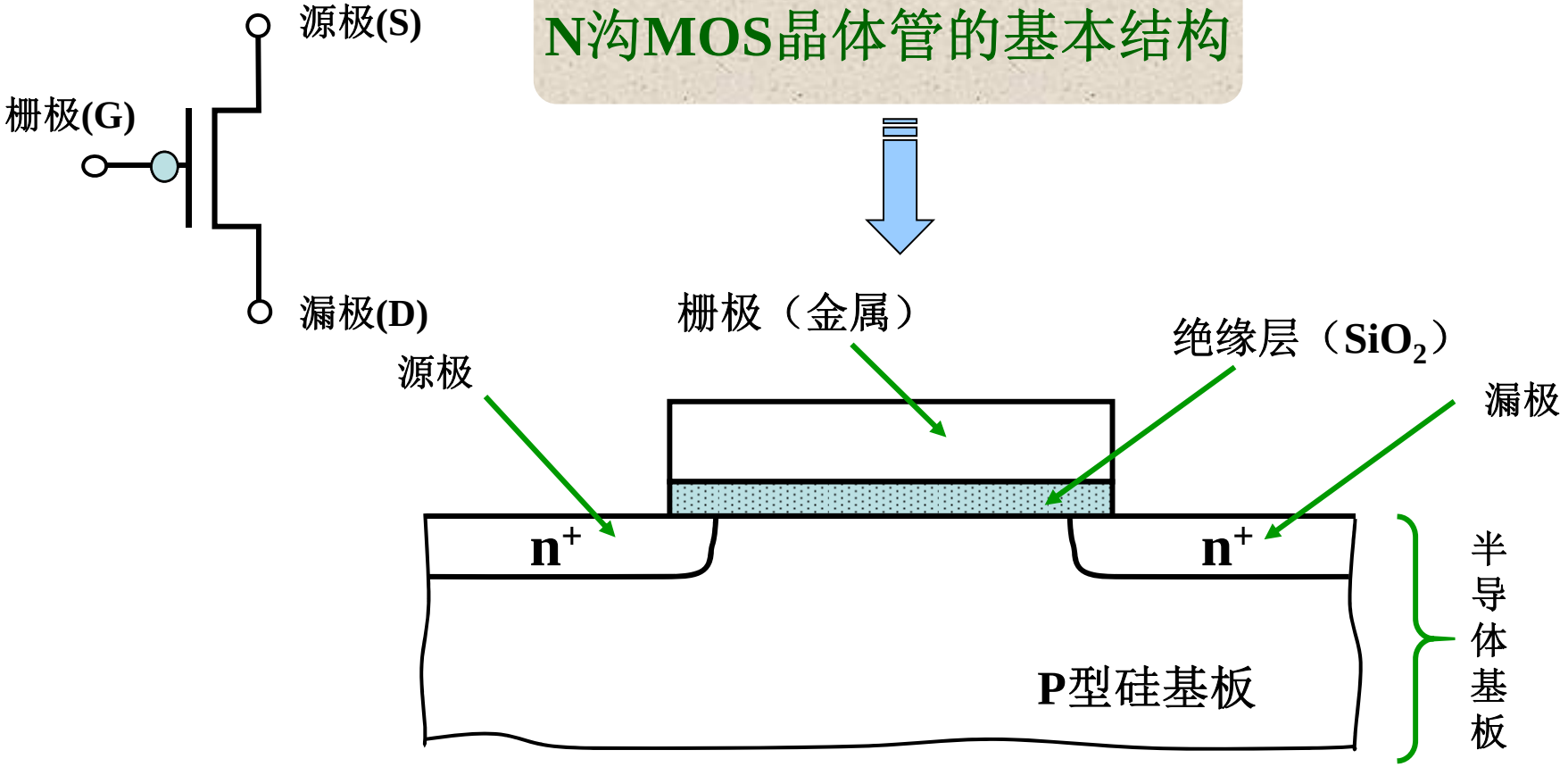



C
E
B
S

本节课内容

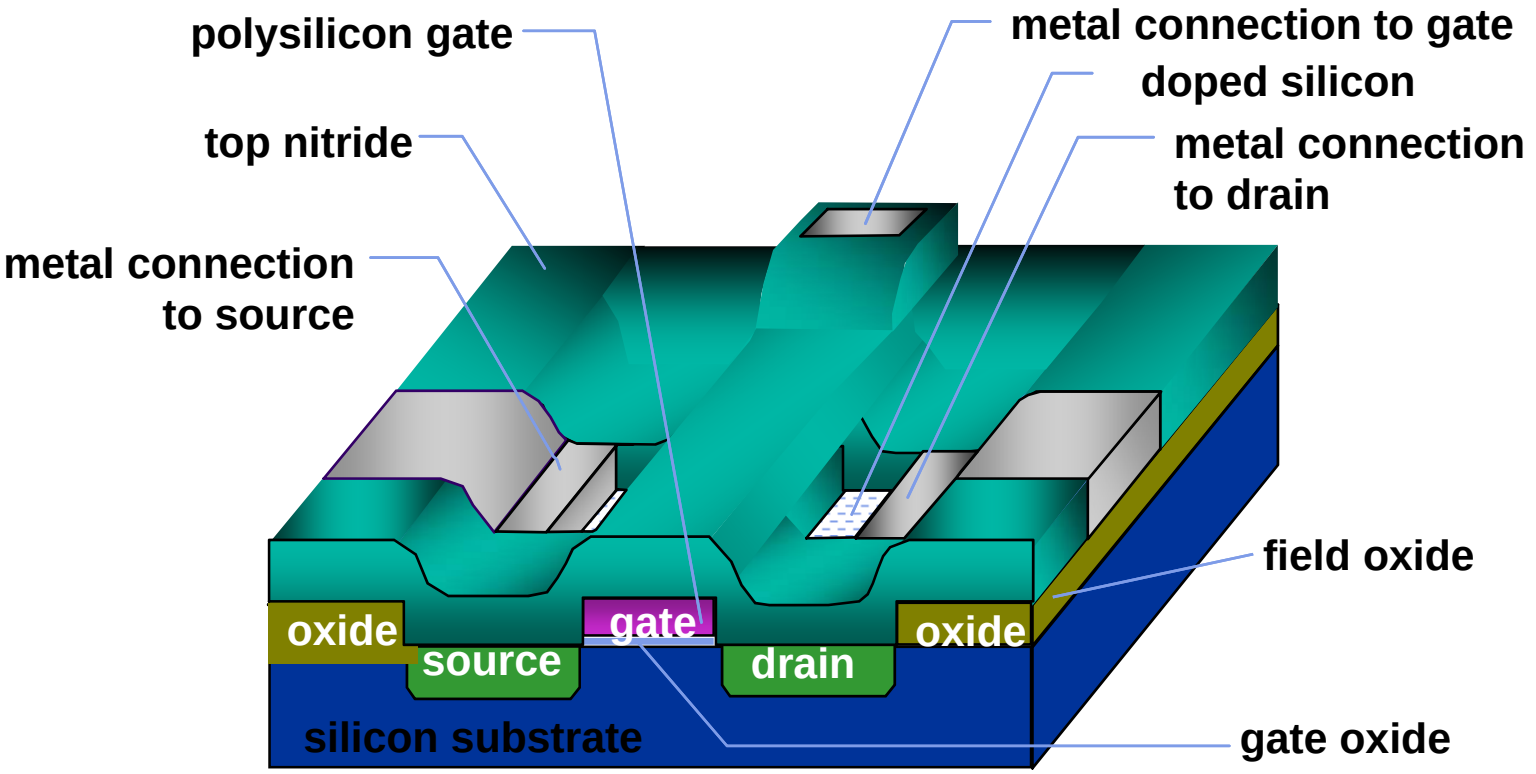
- MOS集成电路的工艺
  - P阱CMOS工艺
  - N阱CMOS工艺
  - 双阱CMOS工艺
- BiCMOS集成电路的工艺

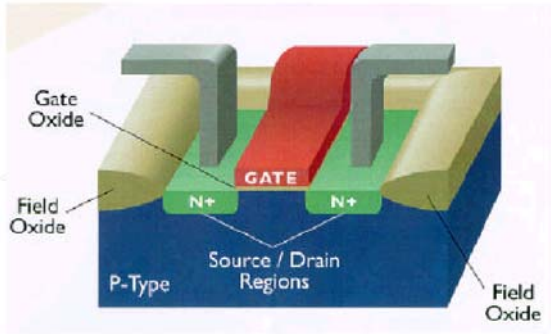
MOSFET的基本结构



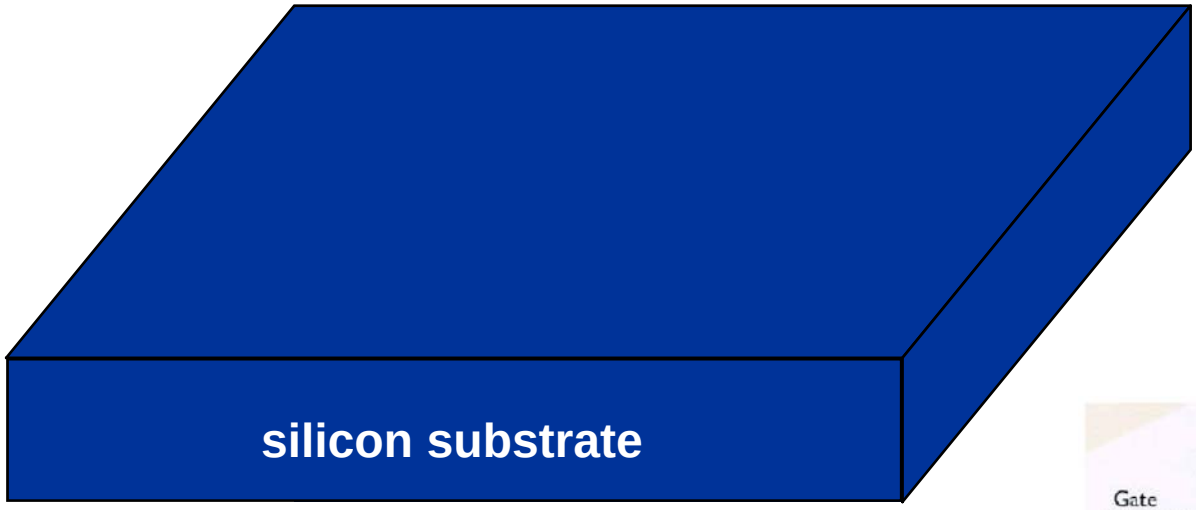
MOS晶体管的动作 ⇒ MOS晶体管实质上是一种使电流时而流过，时而切断的开关

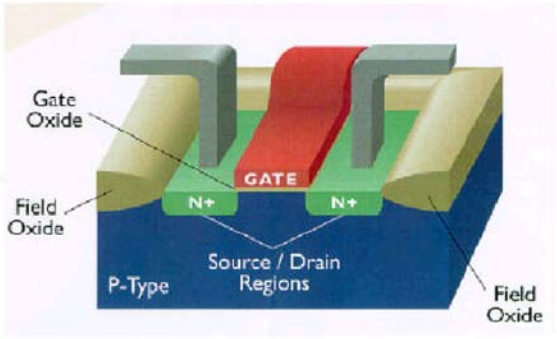
MOS晶体管的立体结构

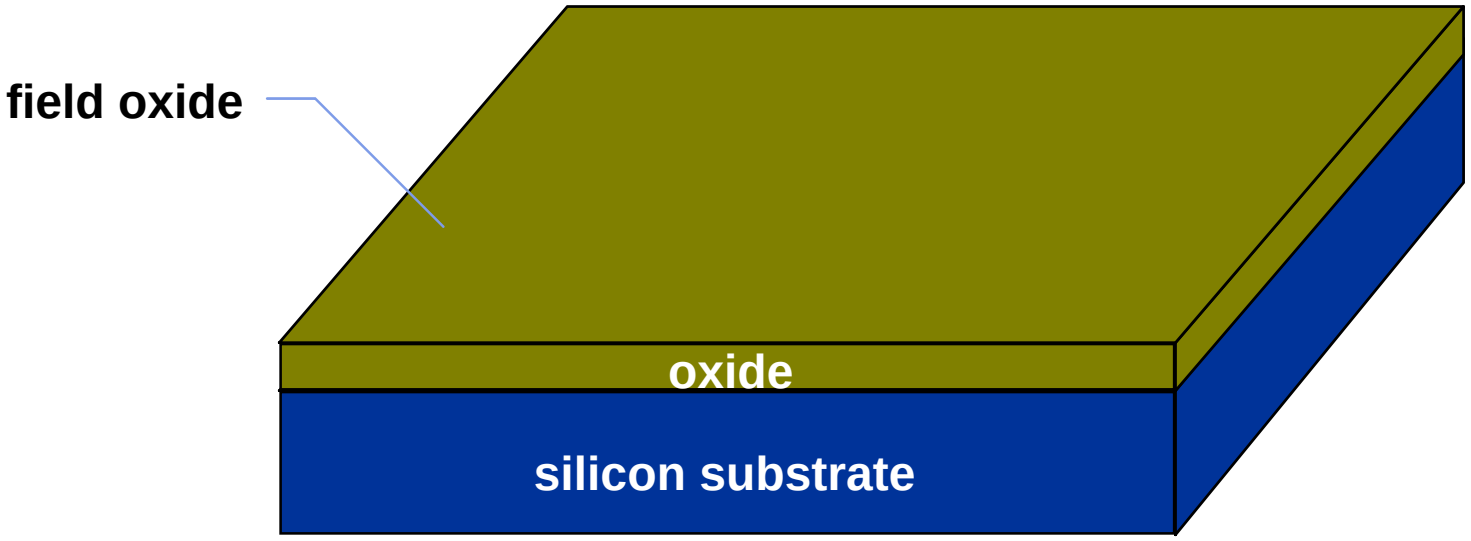


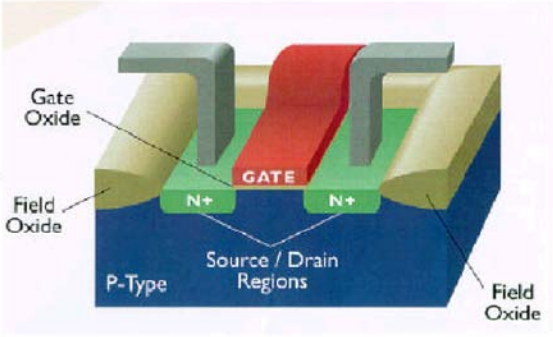


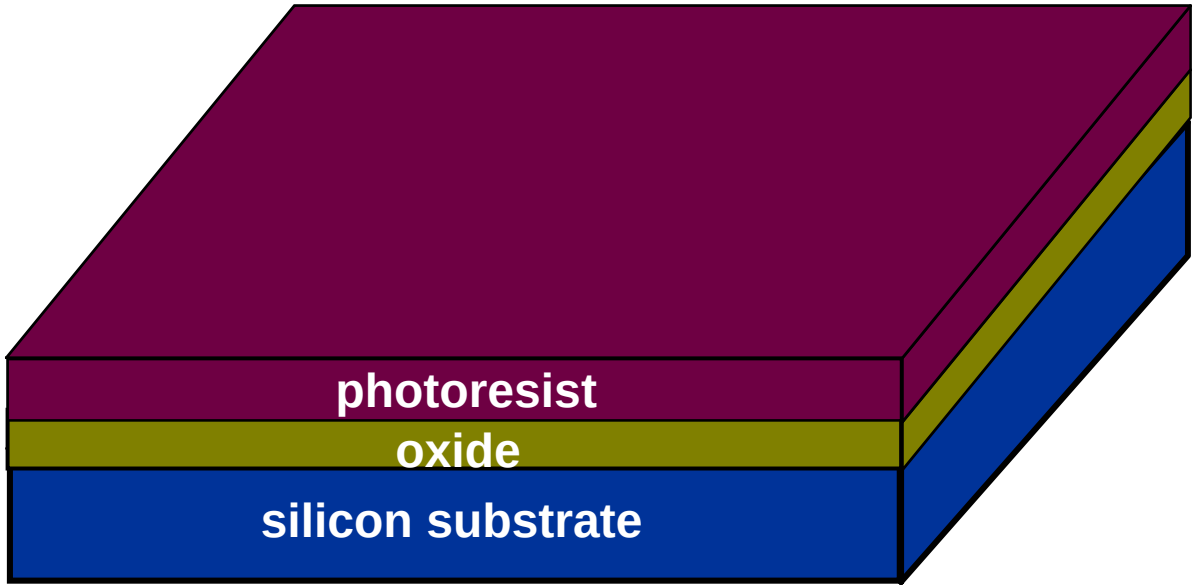
在硅衬底上制作MOS晶体管

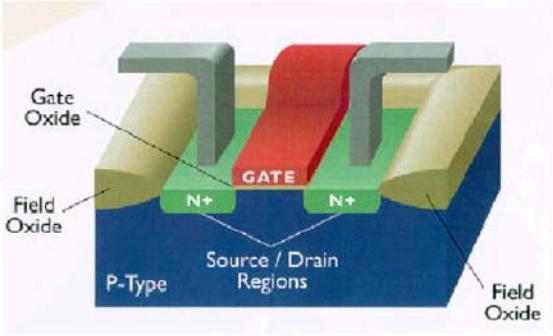


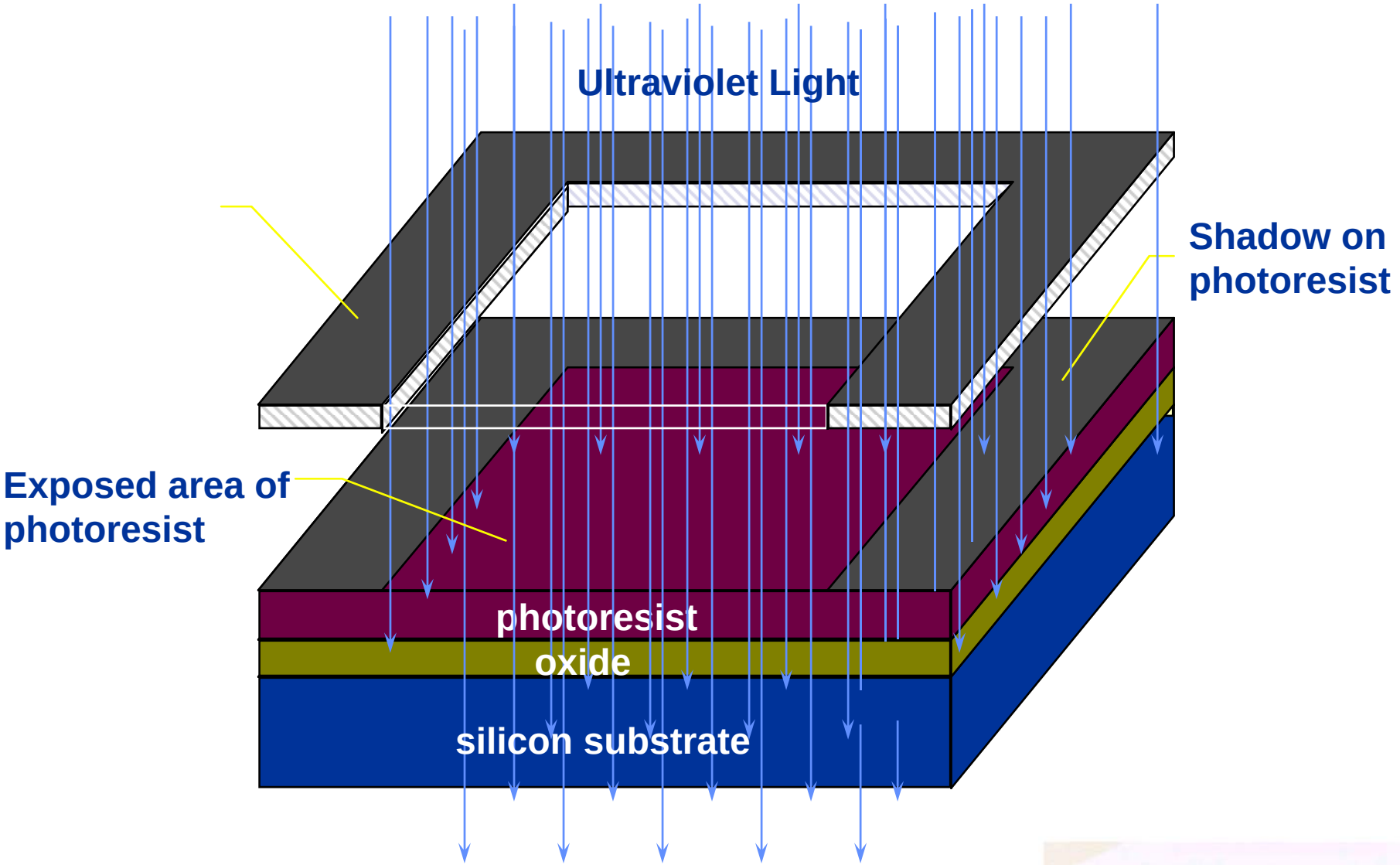


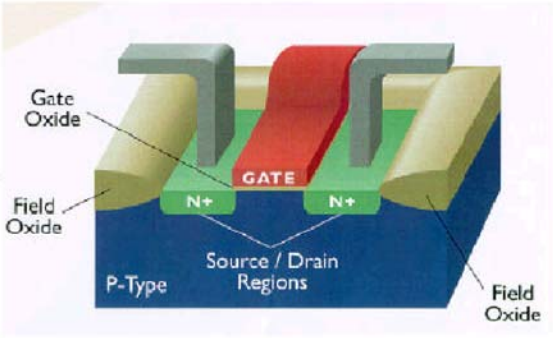

field oxide
oxide
silicon substrate


Gate
Oxide
Field
Oxide
GATE
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide


photoresist
oxide
silicon substrate

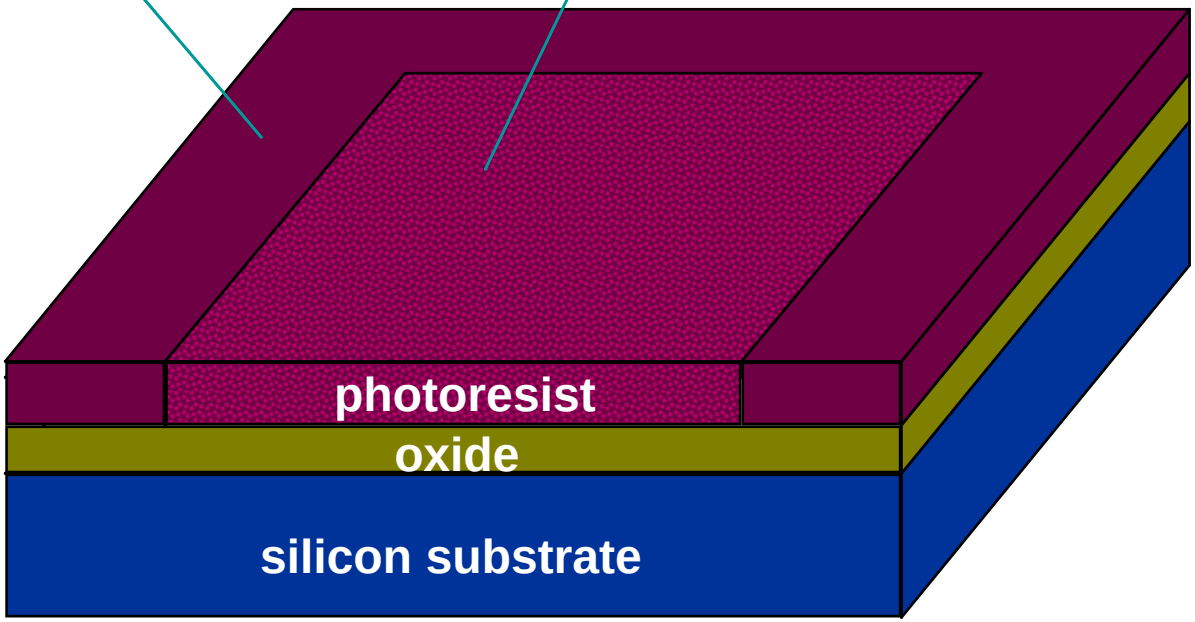

Gate
Oxide
GATE
Field
Oxide
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

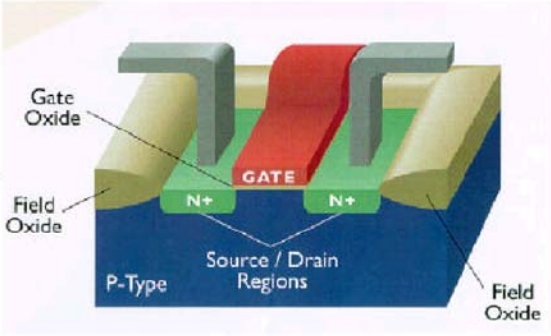

Ultraviolet Light
Shadow on photoresist
Exposed area of photoresist
photoresist
oxide
silicon substrate


Gate Oxide
GATE
N+
N+
Field Oxide
Source / Drain Regions
P-Type
Field Oxide

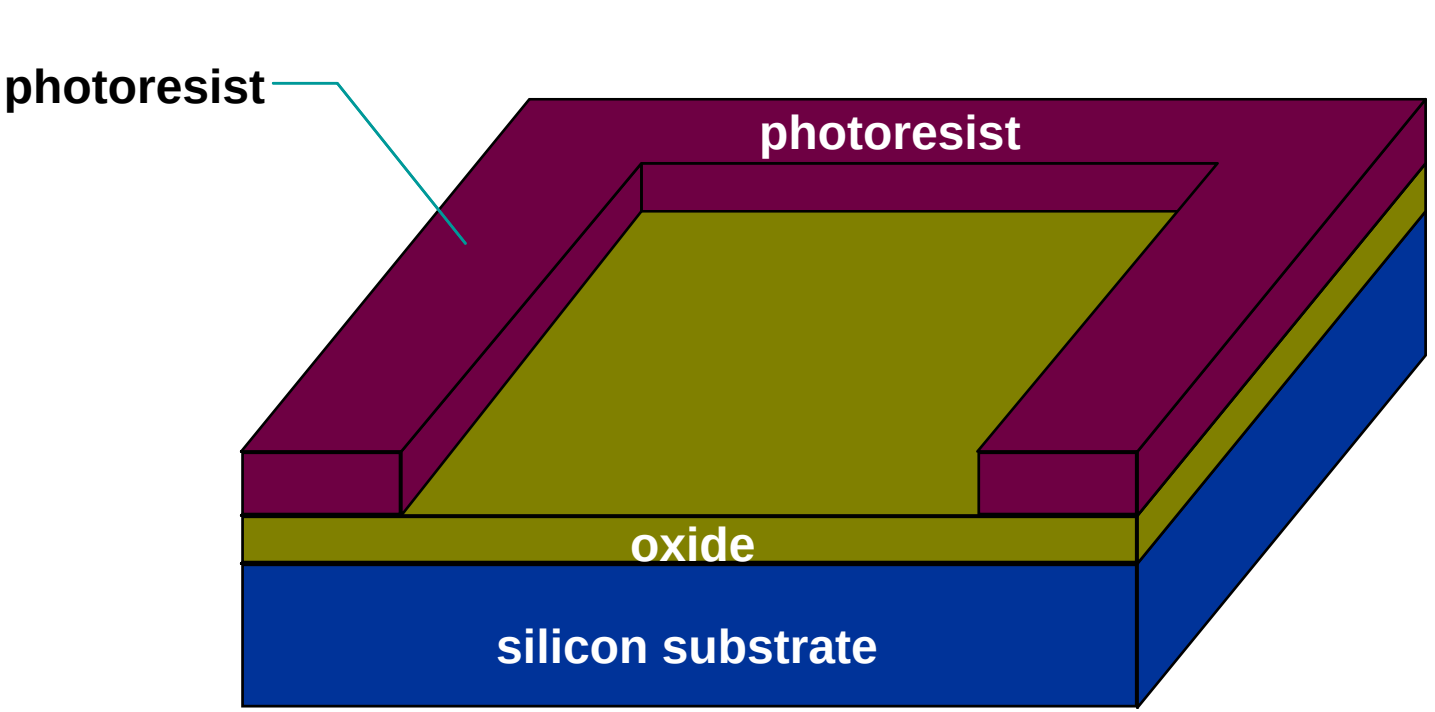
非感光区域

感光区域

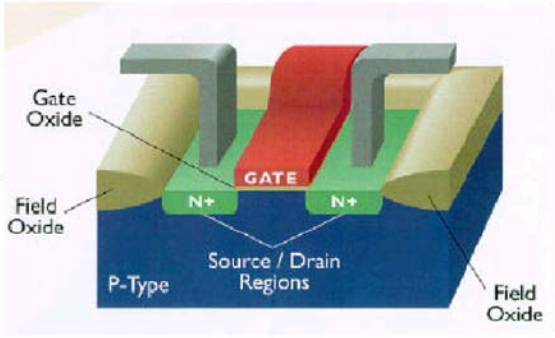

photoresist
oxide
silicon substrate


Gate
Oxide
GATE
N+
N+
Field
Oxide
Source / Drain
Regions
P-Type
Field
Oxide

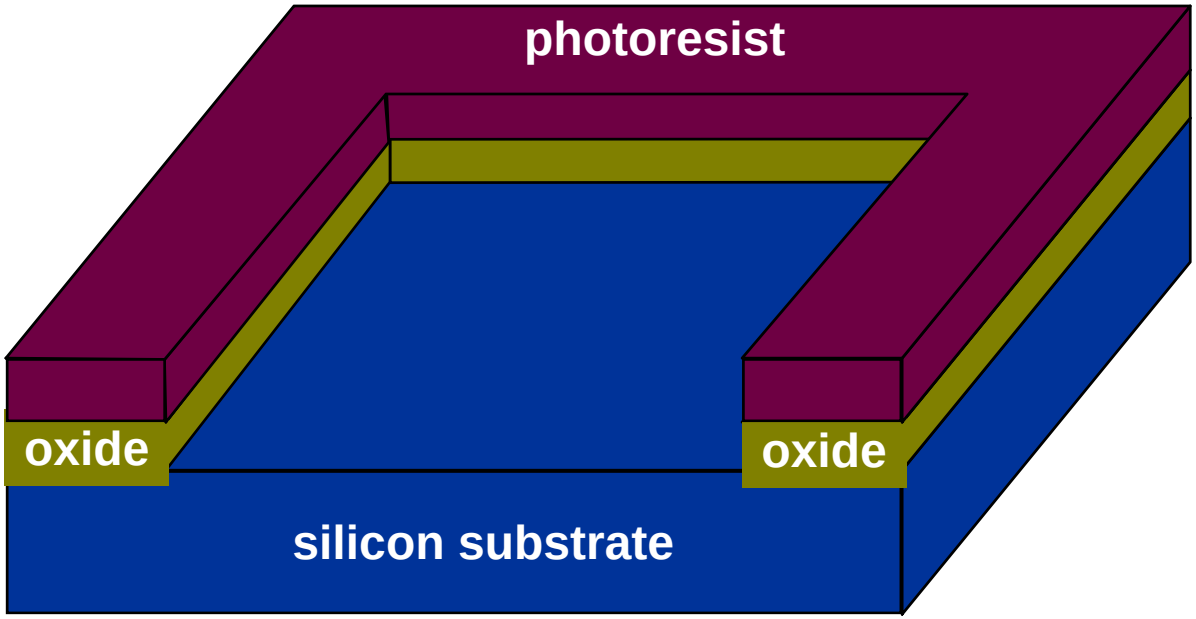
显影

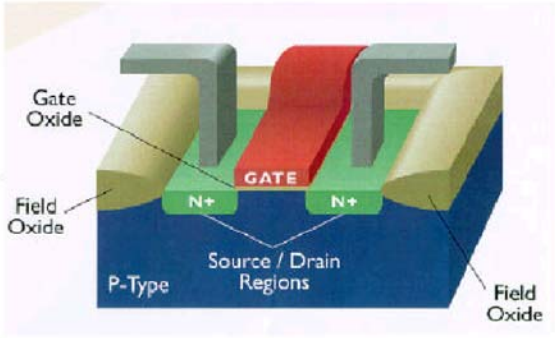


Shadow on photoresist

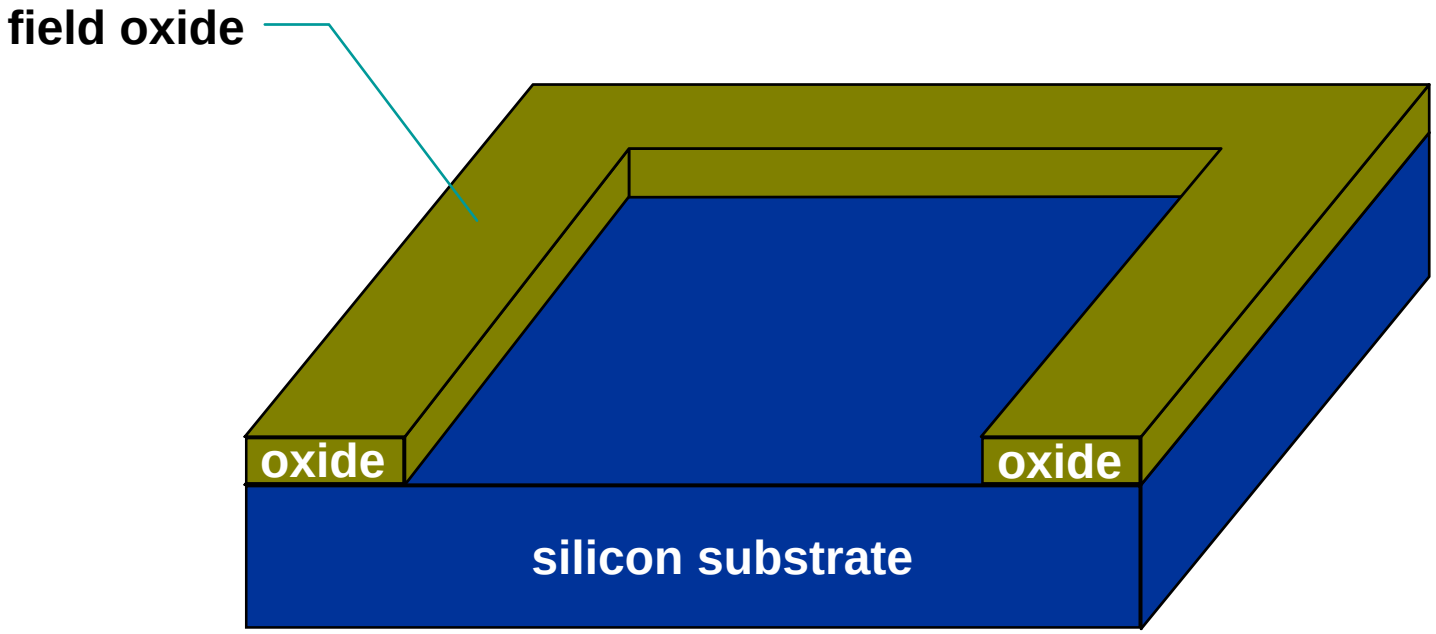


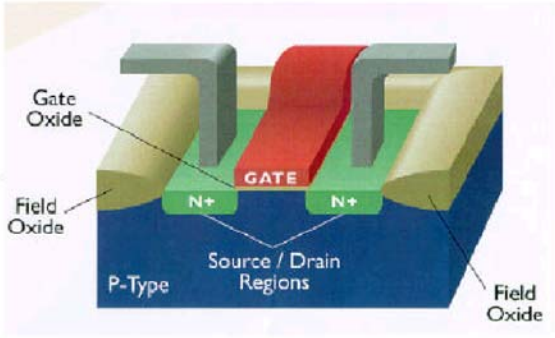
腐蚀

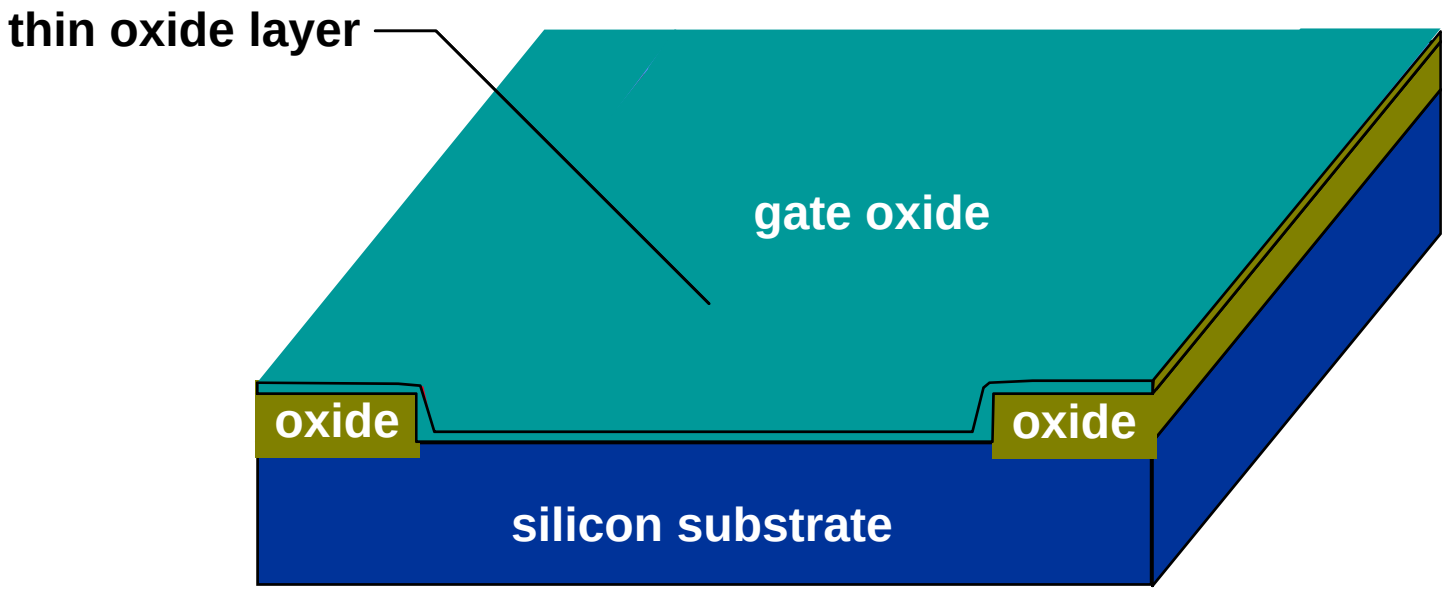

photoresist
oxide
oxide
silicon substrate

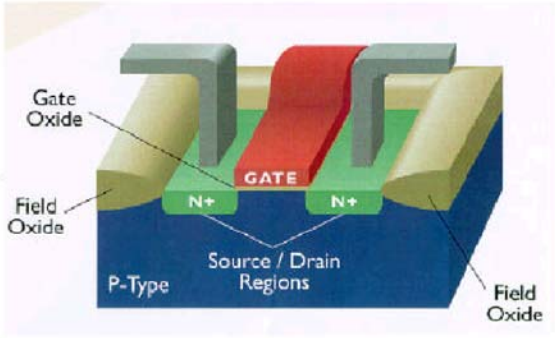

Gate
Oxide
GATE
Field
Oxide
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

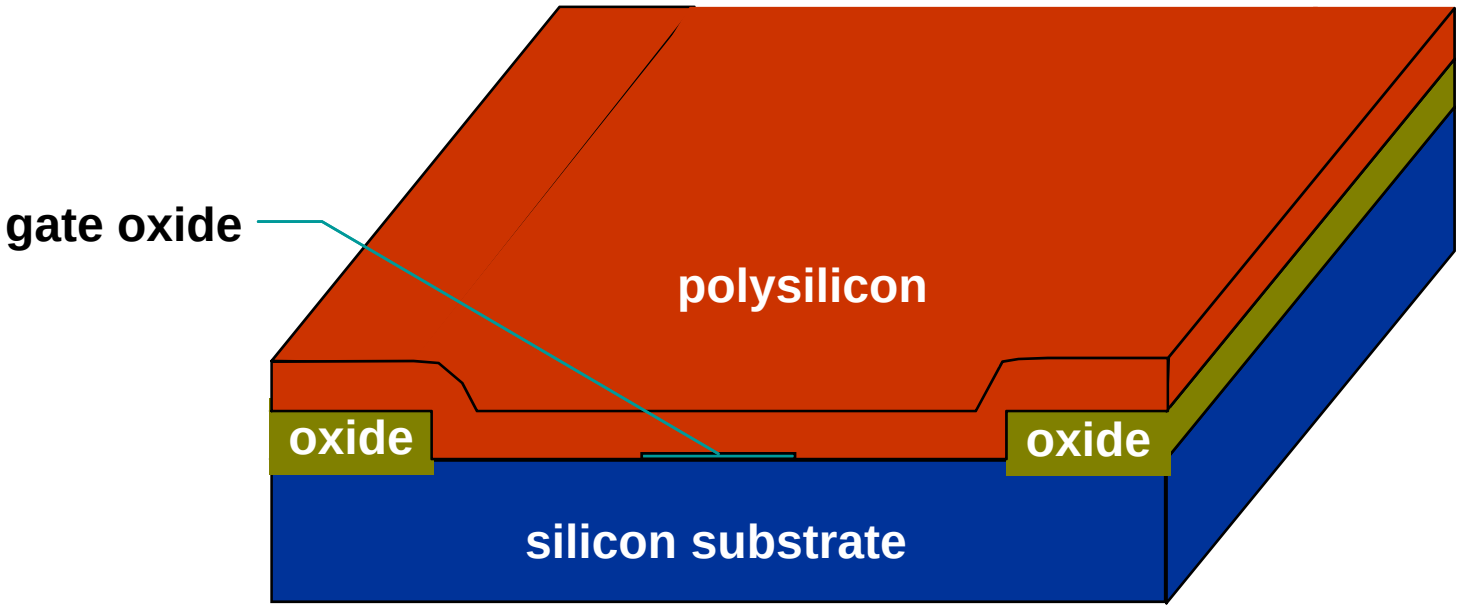
去胶

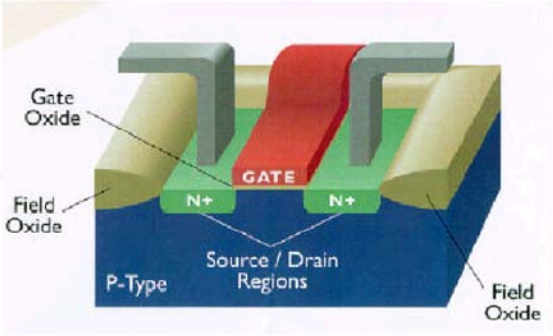

field oxide
oxide
oxide
silicon substrate

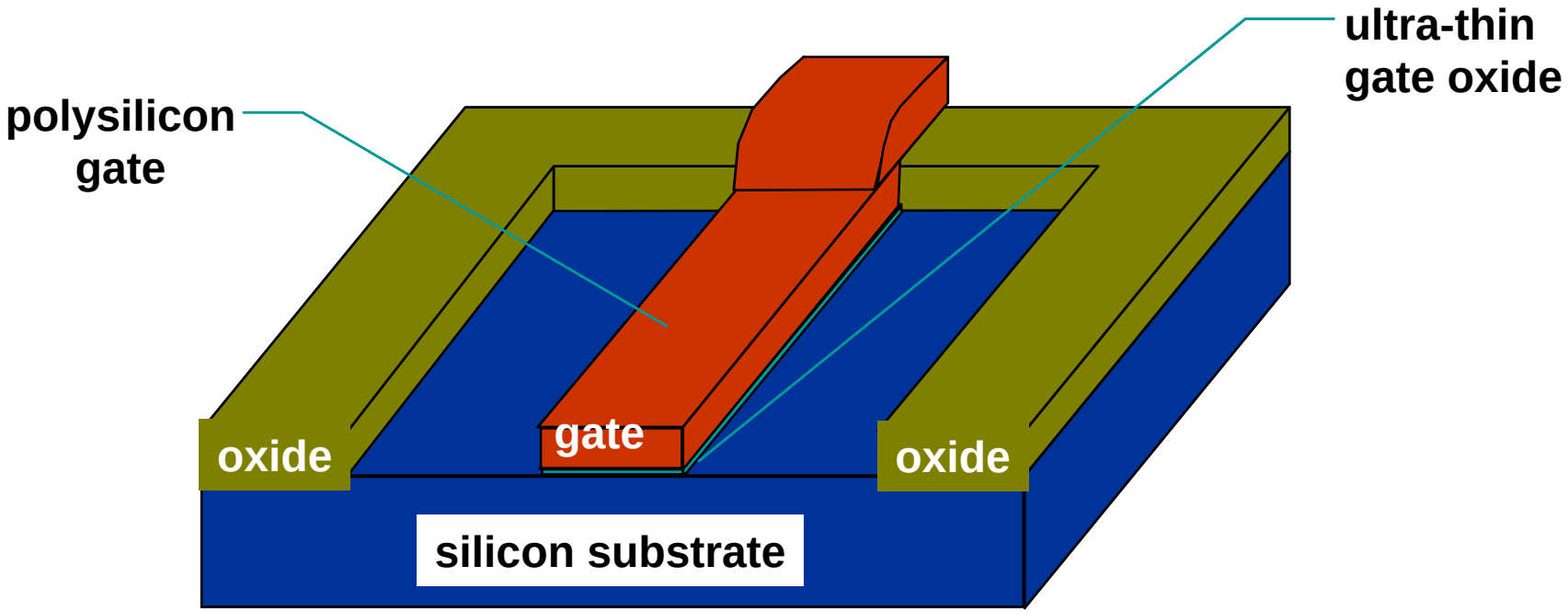

Gate
Oxide
GATE
N+
N+
Field
Oxide
Source / Drain
Regions
P-Type
Field
Oxide

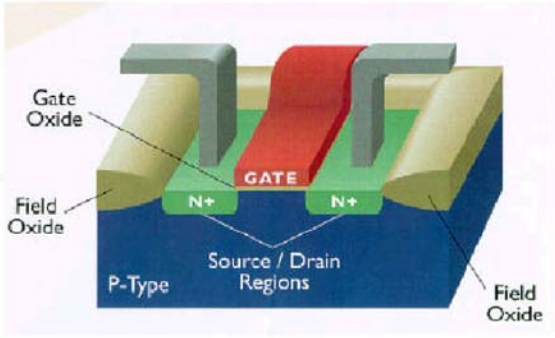

thin oxide layer
gate oxide
oxide
oxide
silicon substrate

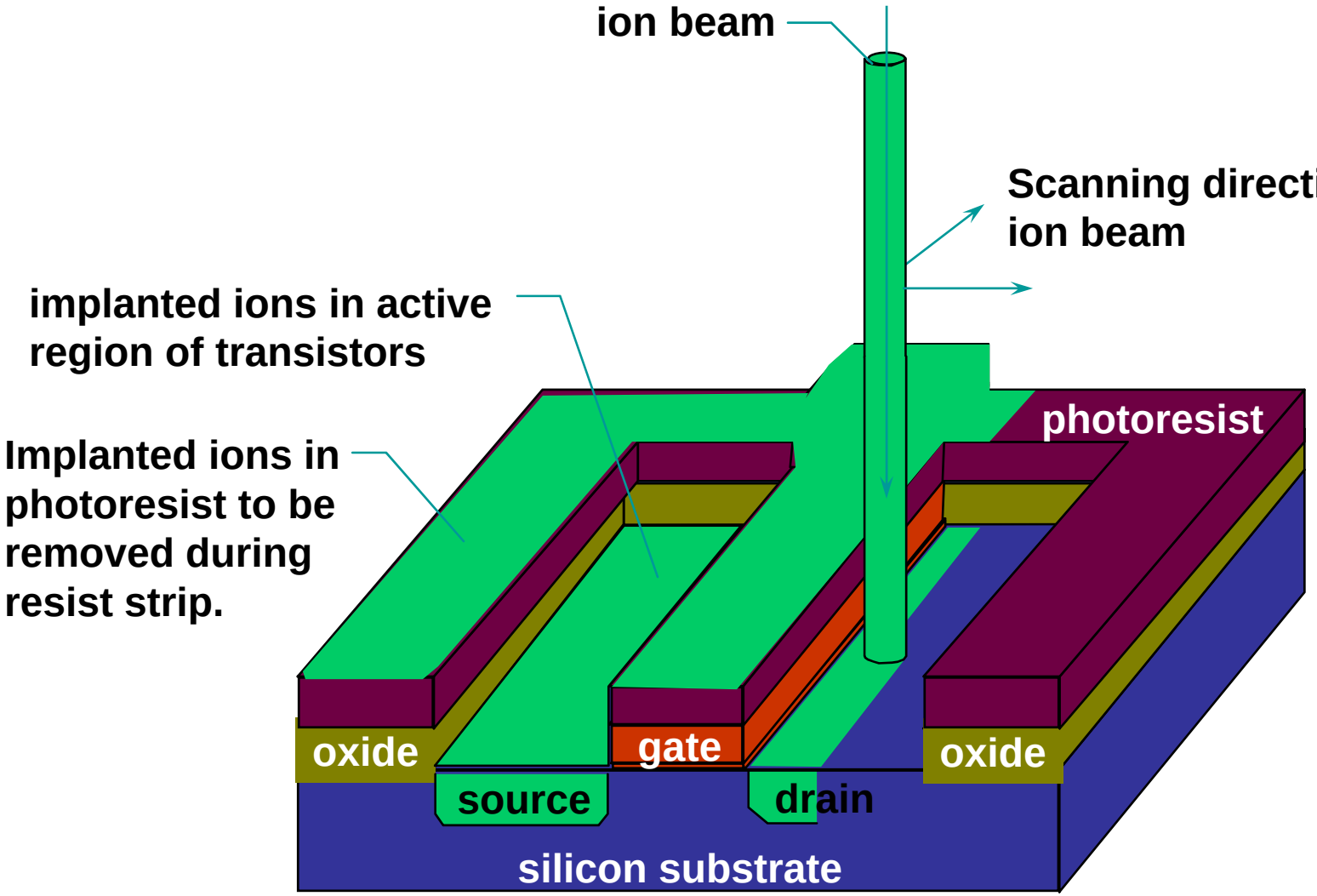

Gate
Oxide
GATE
N+
N+
Field
Oxide
Source / Drain
Regions
P-Type
Field
Oxide

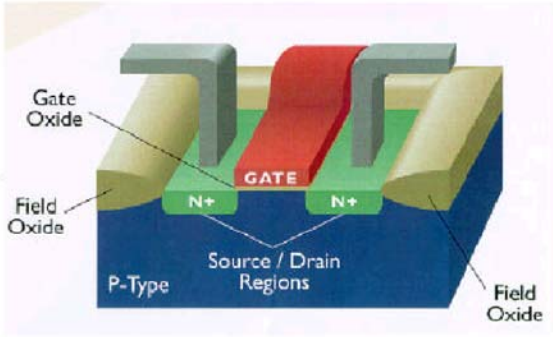

gate oxide
polysilicon
oxide
oxide
silicon substrate

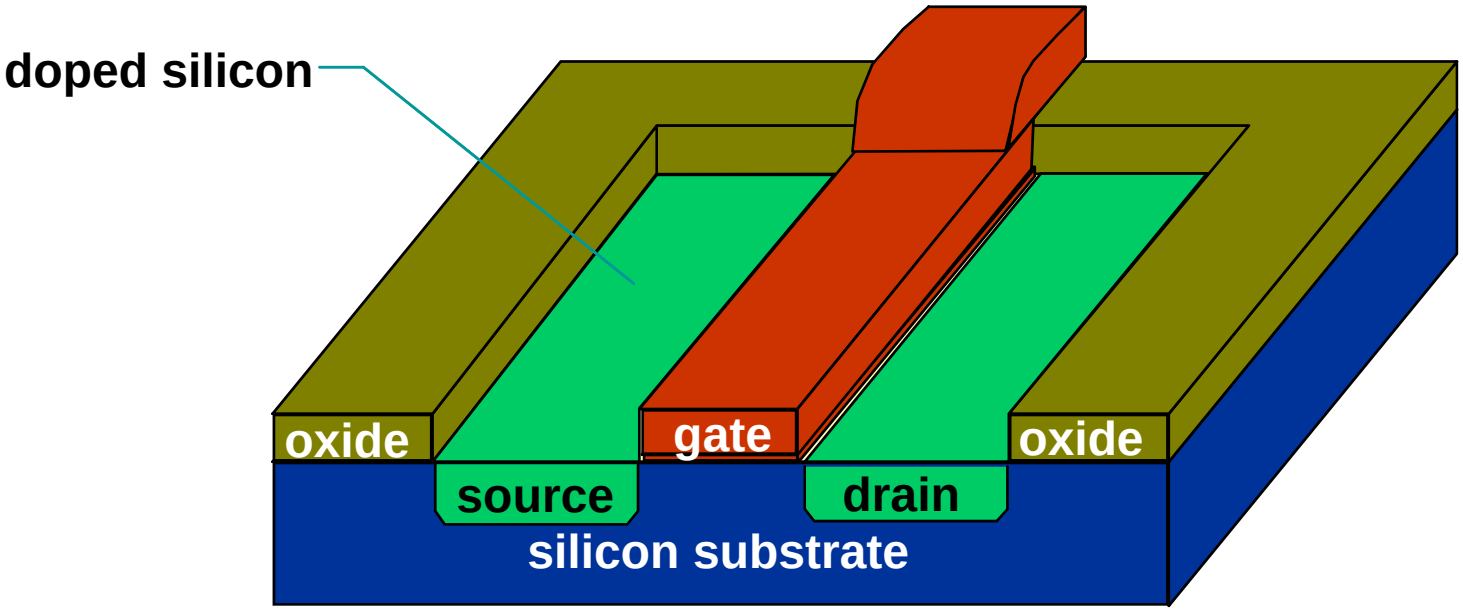

Gate
Oxide
GATE
Field
Oxide
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

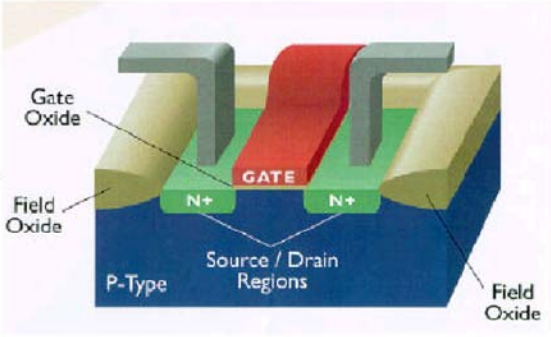

polysilicon
gate
ultra-thin
gate oxide
oxide
gate
oxide
silicon substrate


Gate
Oxide
GATE
Field
Oxide
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide


ion beam
Scanning direction of ion beam
implanted ions in active region of transistors
Implanted ions in photoresist to be removed during resist strip.
photoresist
oxide
gate
oxide
source
drain
silicon substrate

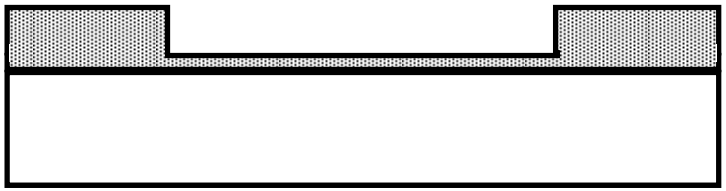

Gate Oxide
GATE
Field Oxide
N+
N+
Source / Drain Regions
P-Type
Field Oxide


doped silicon
oxide
gate
oxide
source
drain
silicon substrate

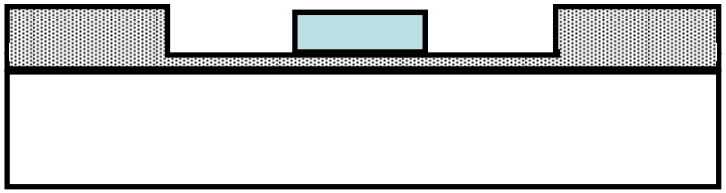

Gate
Oxide
GATE
Field
Oxide
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

自对准工艺

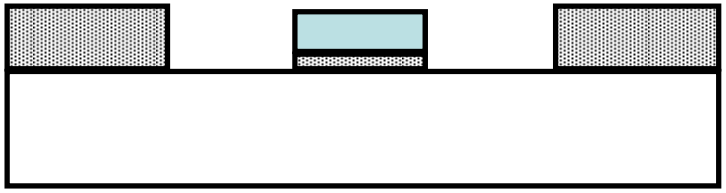
1. 在有源区上覆盖一层薄氧化层



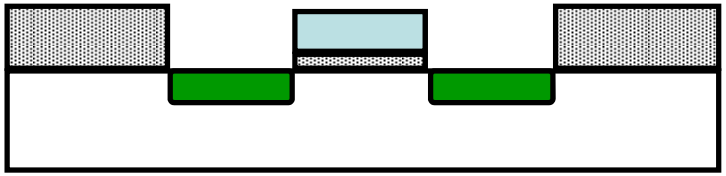
2. 淀积多晶硅，用多晶硅栅极版图刻蚀多晶硅

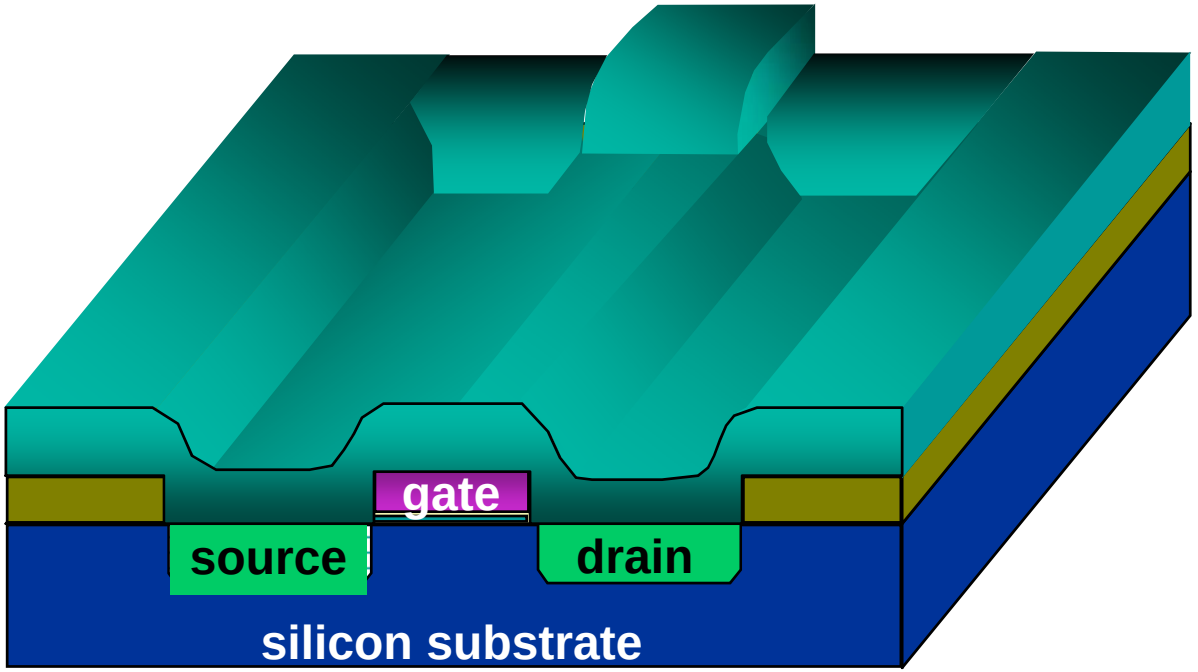


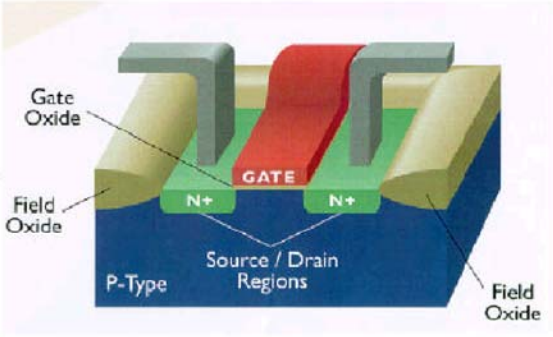
3. 以多晶硅栅极图形为掩膜板，刻蚀氧化膜

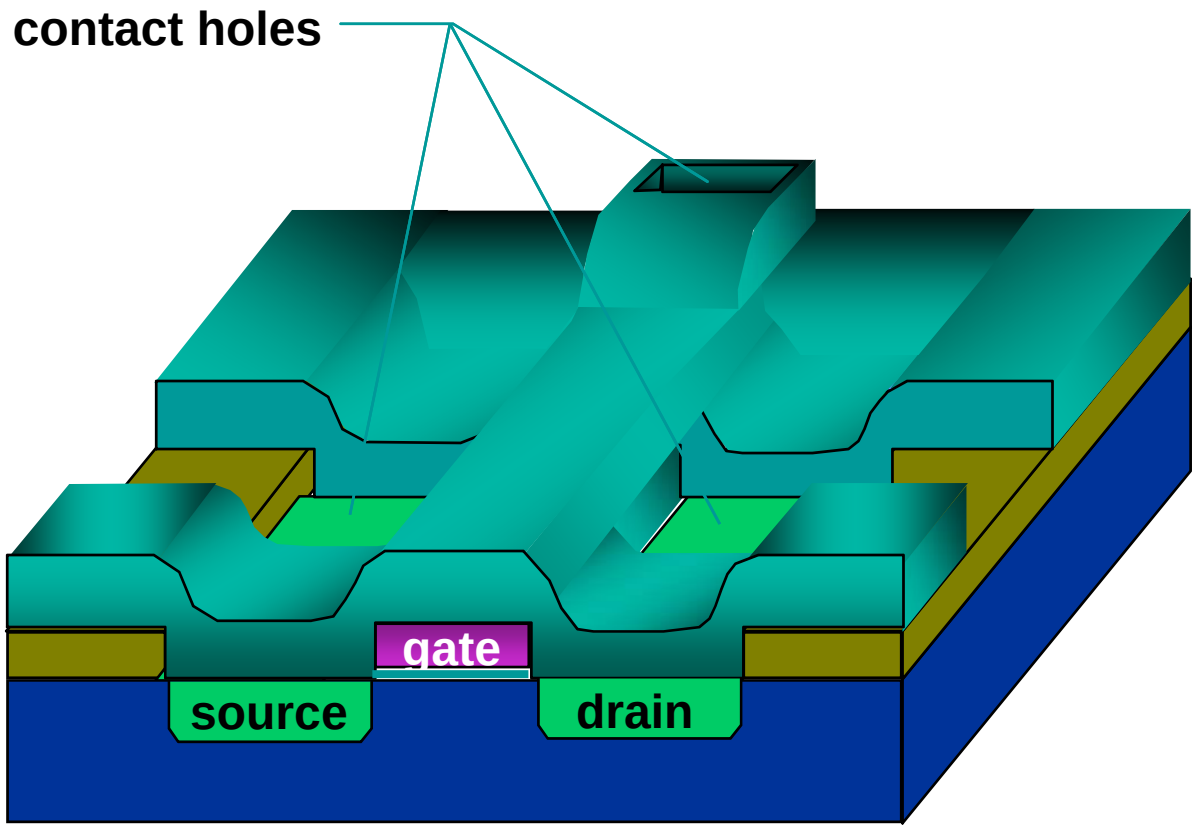


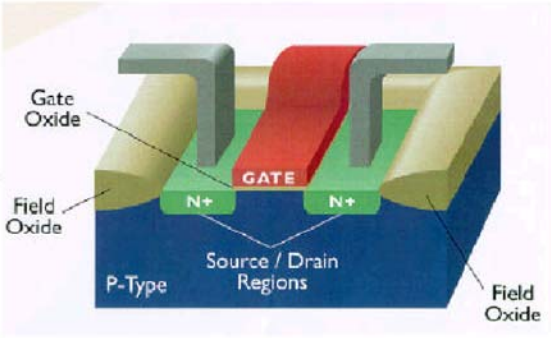
4. 离子注入

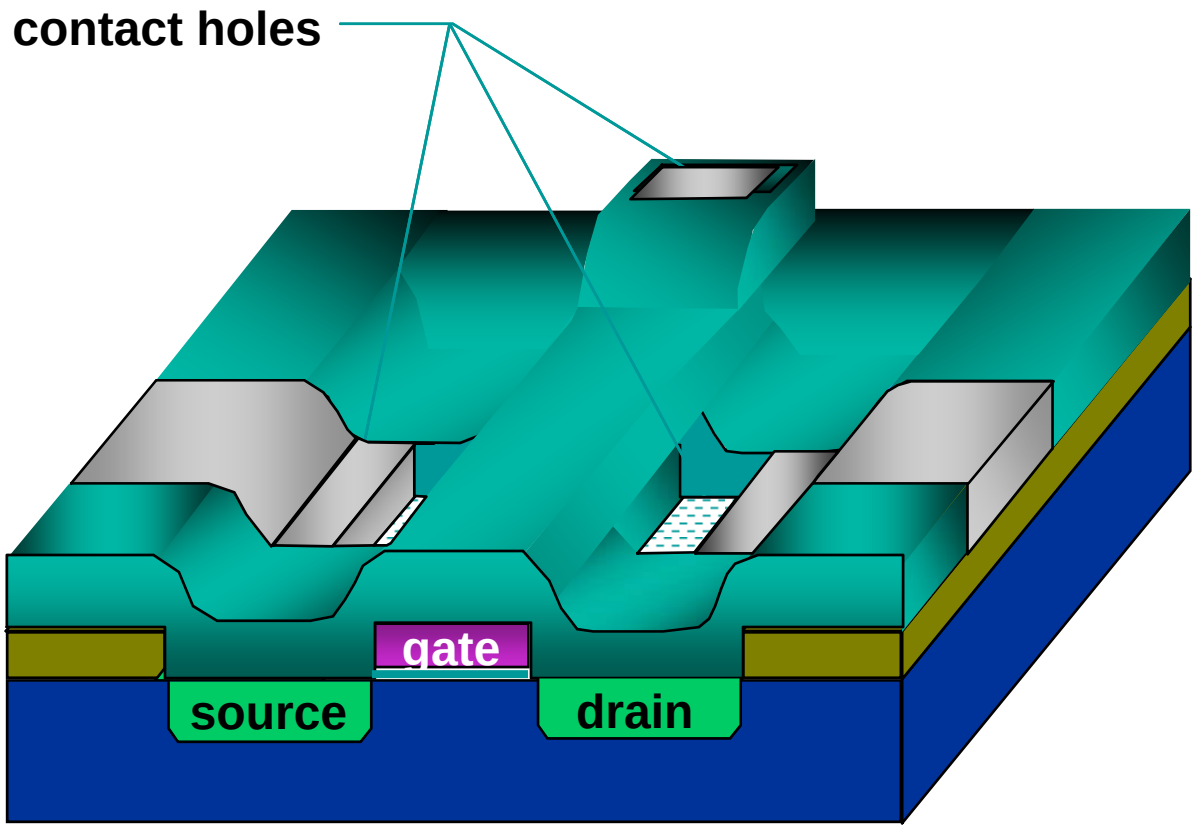


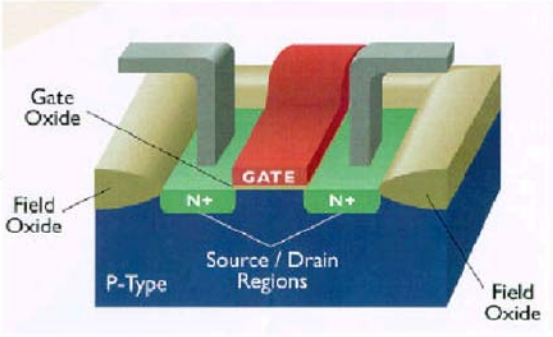

gate
source
drain
silicon substrate


Gate
Oxide
Field
Oxide
GATE
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

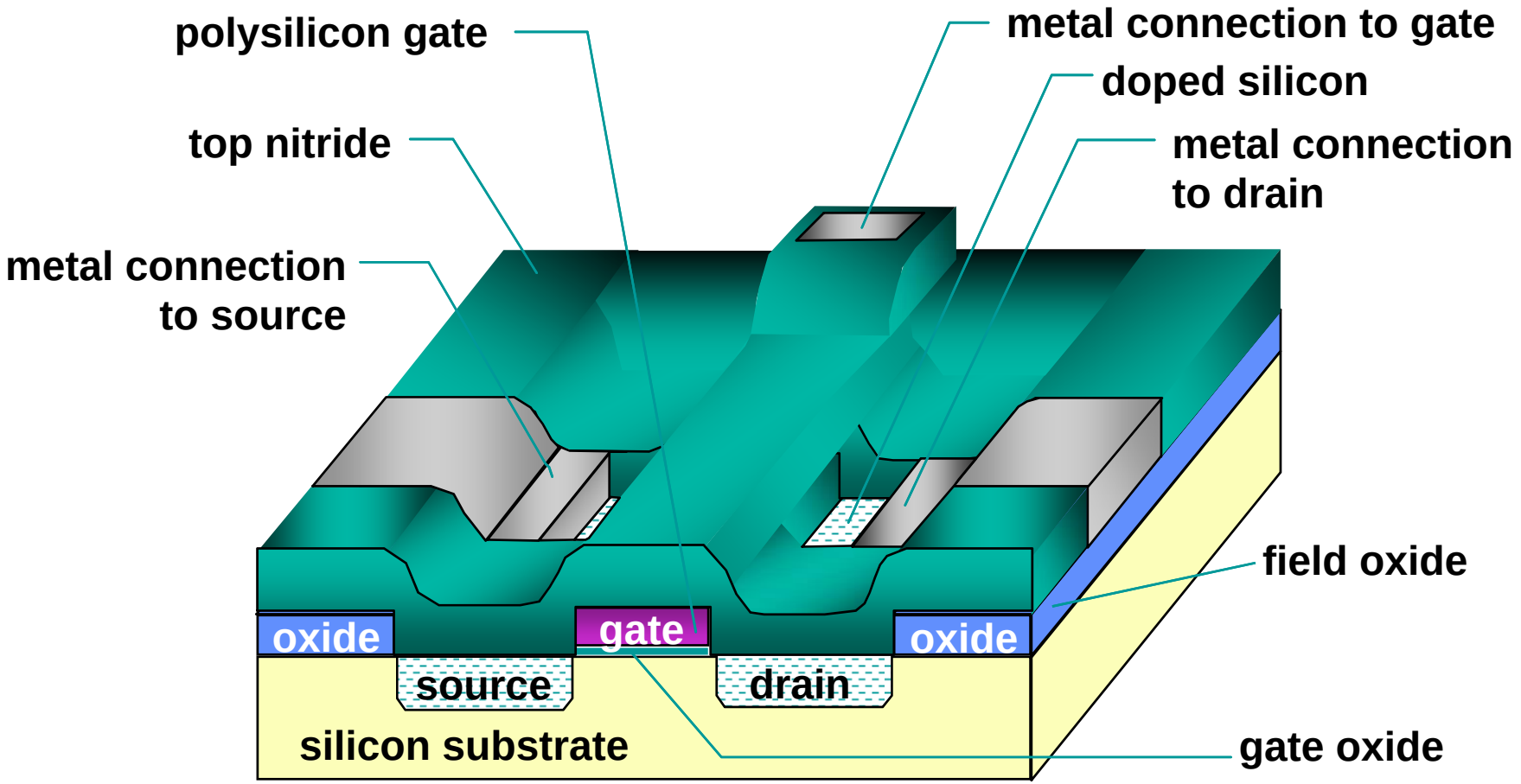

contact holes
gate
source
drain


Gate
Oxide
Field
Oxide
GATE
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

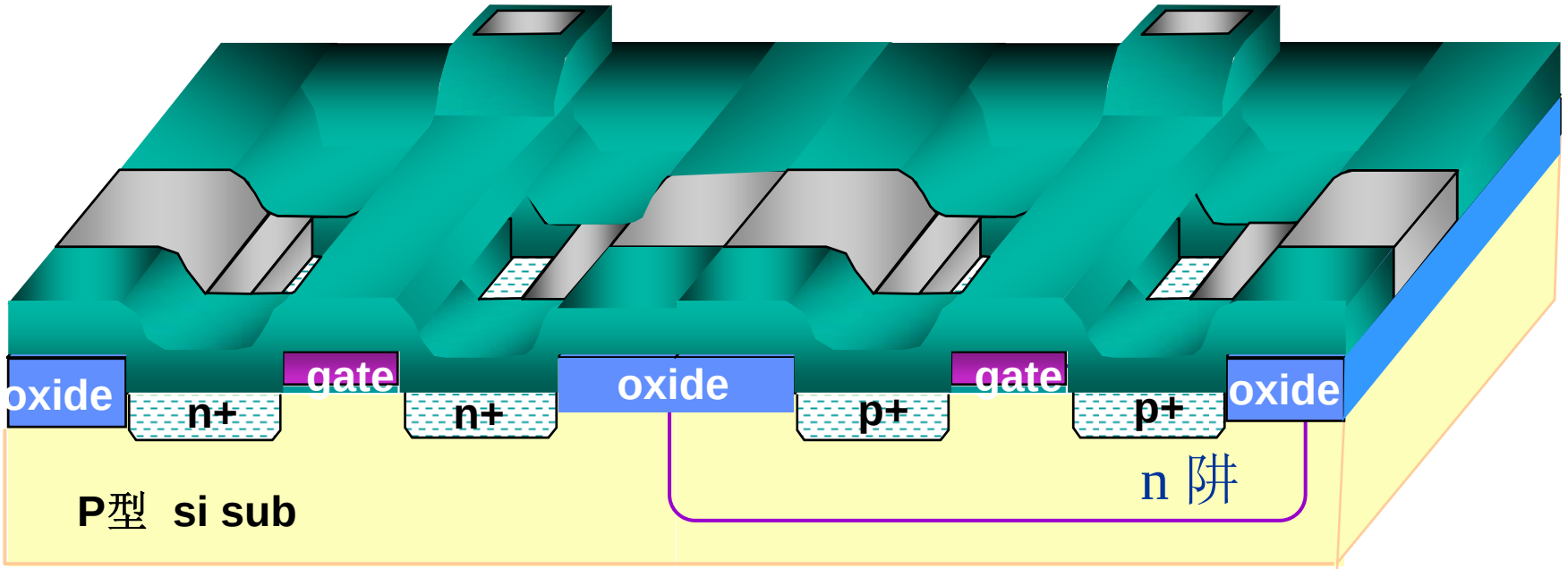

contact holes
gate
source
drain


Gate
Oxide
Field
Oxide
GATE
N+
N+
Source / Drain
Regions
P-Type
Field
Oxide

完整的简单MOS晶体管结构

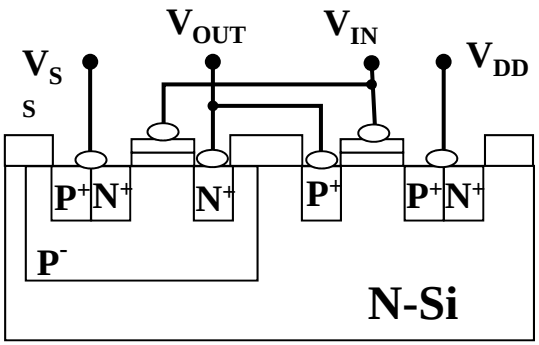


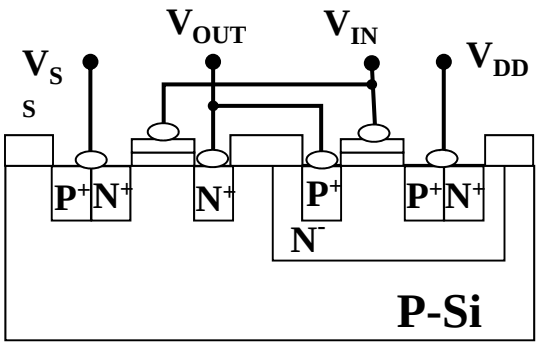
CMOSFET

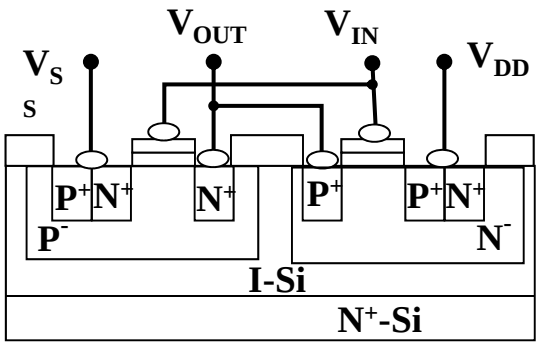


主要的CMOS工艺

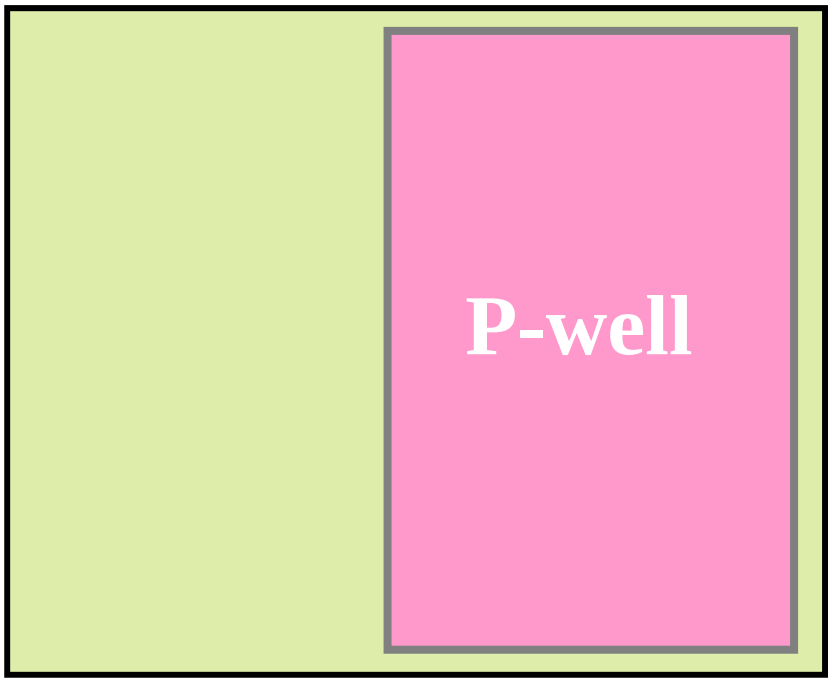
- P阱工艺
- N阱工艺
- 双阱工艺

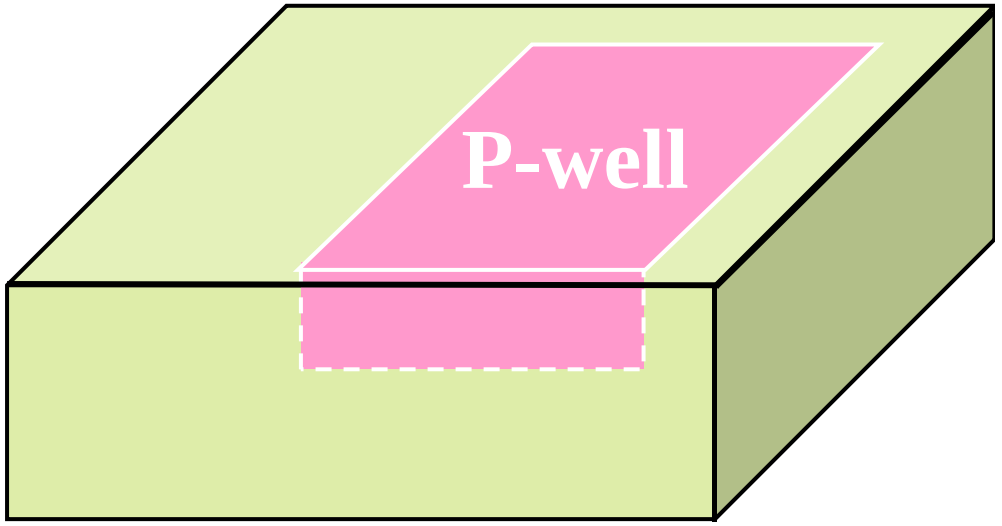


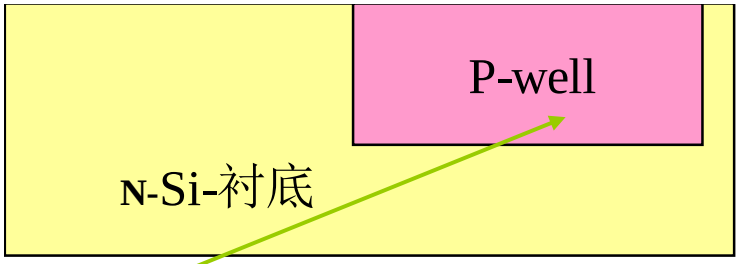


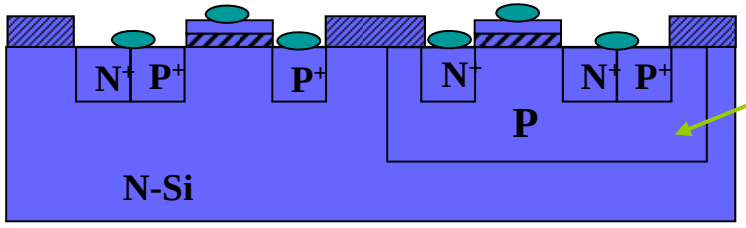


- 掩膜1： P阱光刻



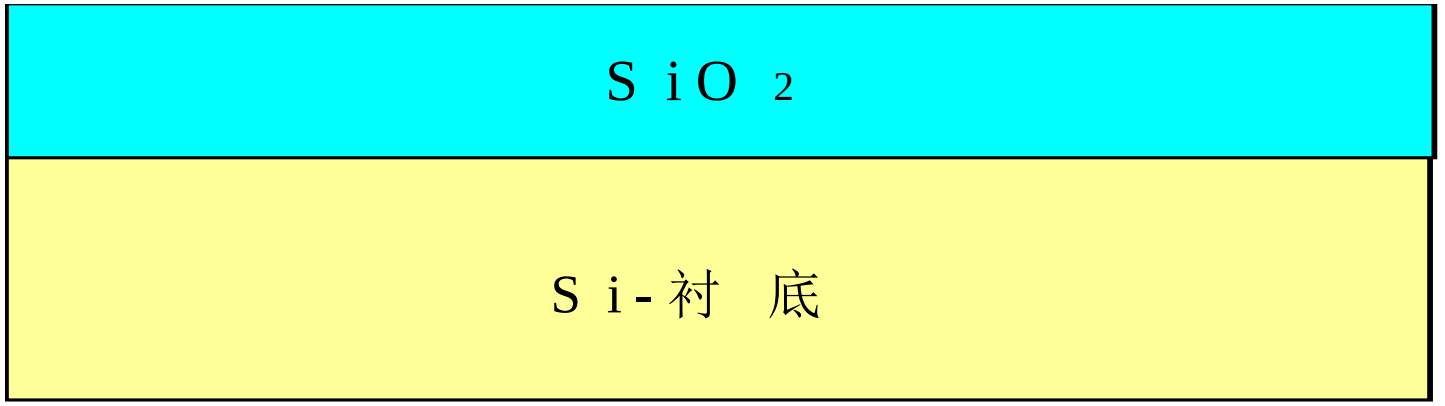






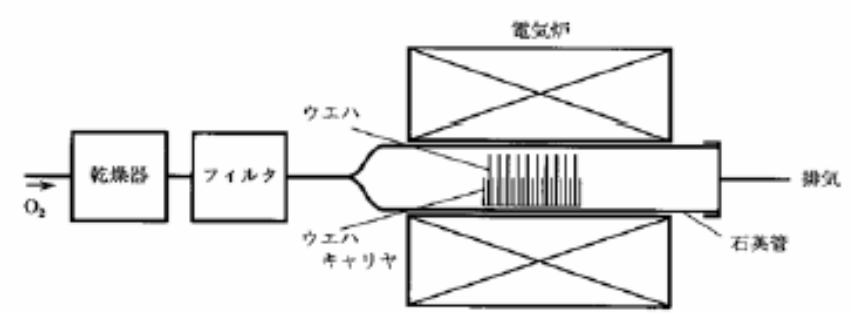
具体步骤如下：

1. 生长二氧化硅（湿法氧化）：

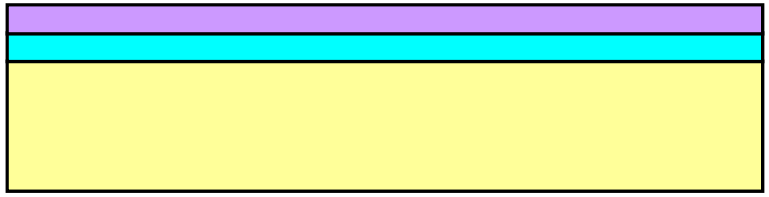


$$Si(\text{固体}) + 2H_2O \rightarrow SiO_2(\text{固体}) + 2H_2$$

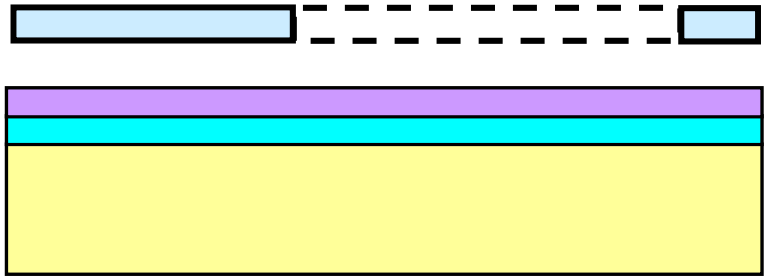
氧　化



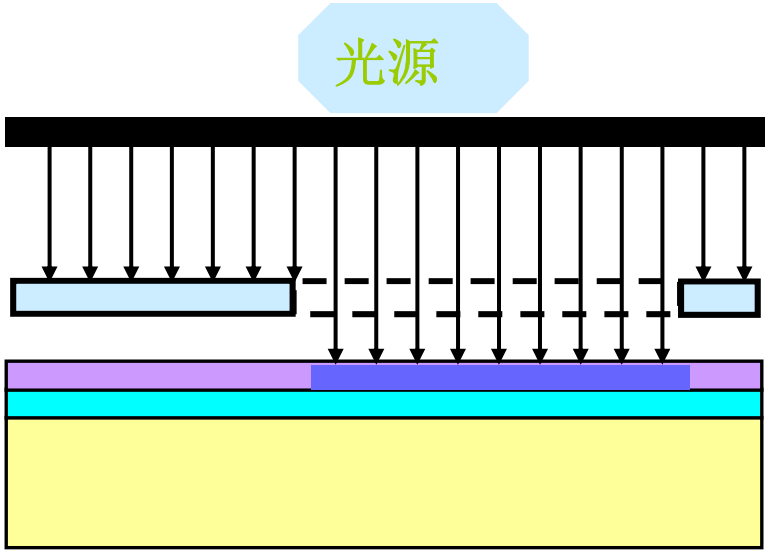
2．P阱光刻：



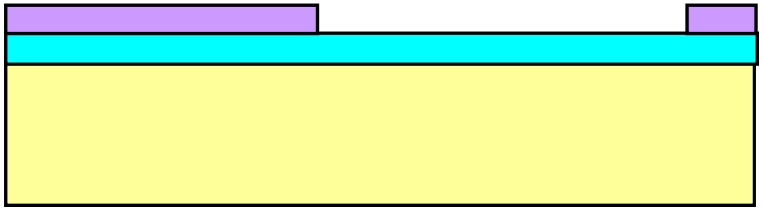
涂胶



掩膜对准



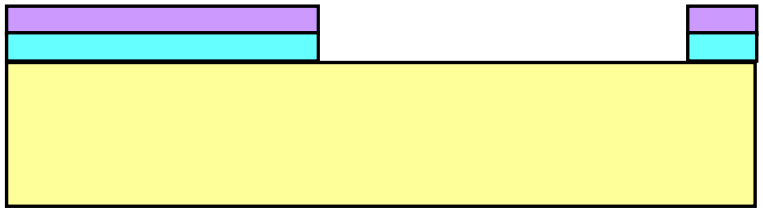
曝光



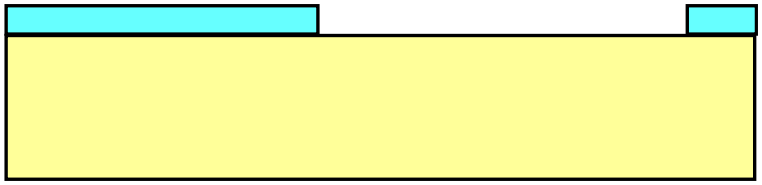
显影

●縮小投影露光装置（ステッパ）

●露光面

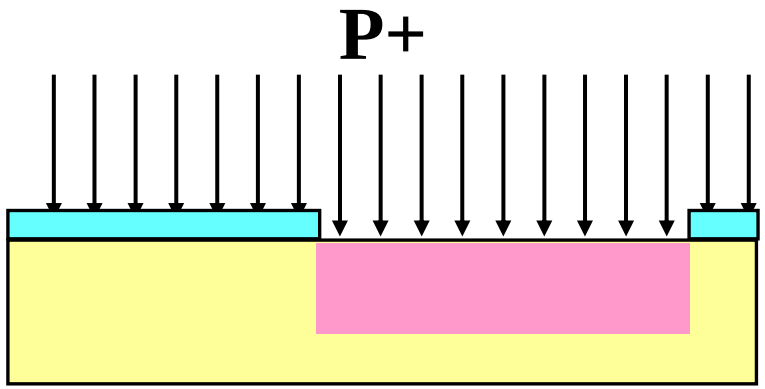


刻蚀（等离子体刻蚀）

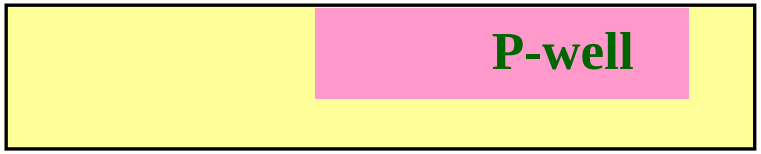


去胶

3．P阱掺杂：

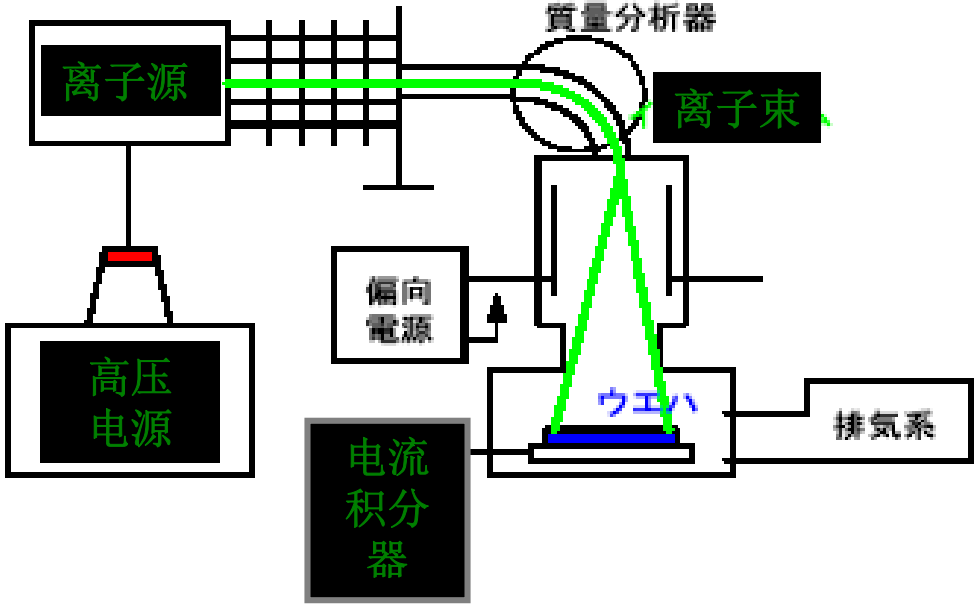


硼掺杂（离子注入）



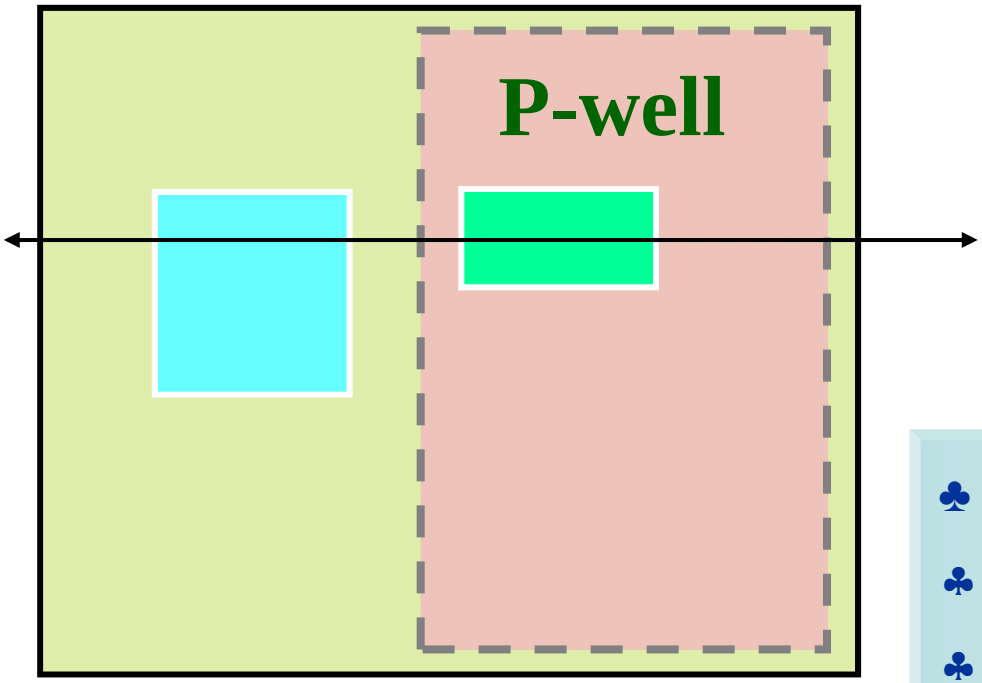
去除氧化膜

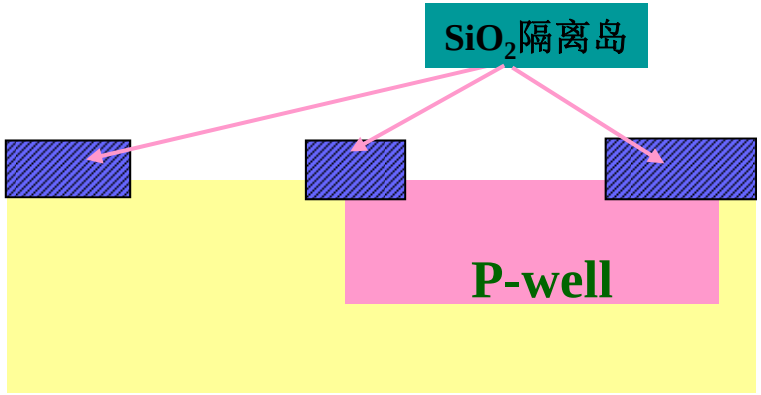
●イオン注入装置内部

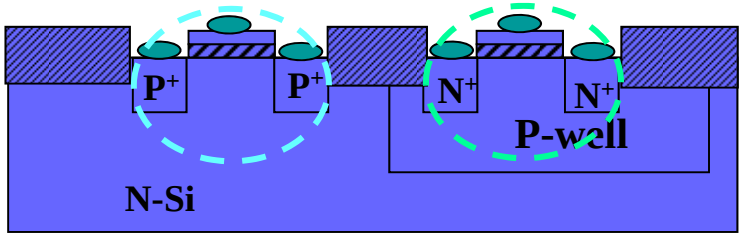


• 掩膜2： 光刻有源区

有源区：**nMOS、PMOS**
晶体管形成的区域

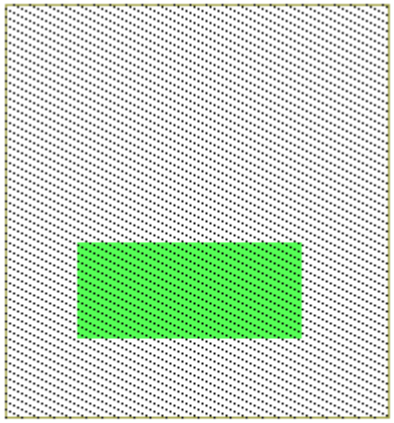






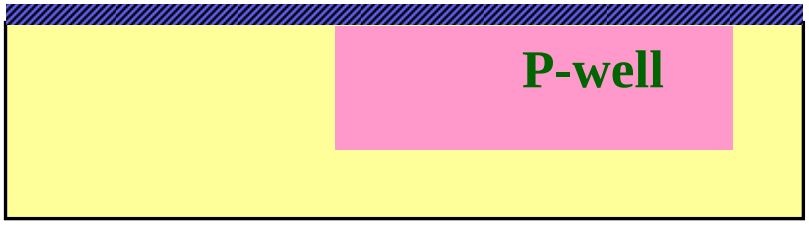
- ♣ 淀积氮化硅
- ♣ 光刻有源区
- ♣ 场区氧化
- ♣ 去除有源区氮化硅及二氧化硅

有源区

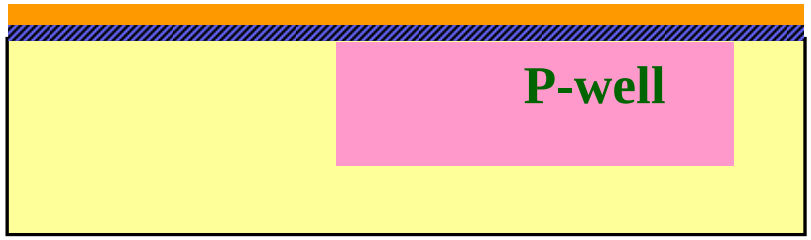


有源区光刻板
N型p型MOS制作区域
(漏-栅-源)

1. 淀积氮化硅：

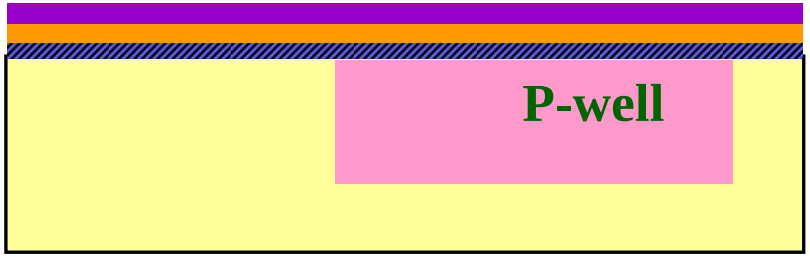


氧化膜生长（湿法氧化）



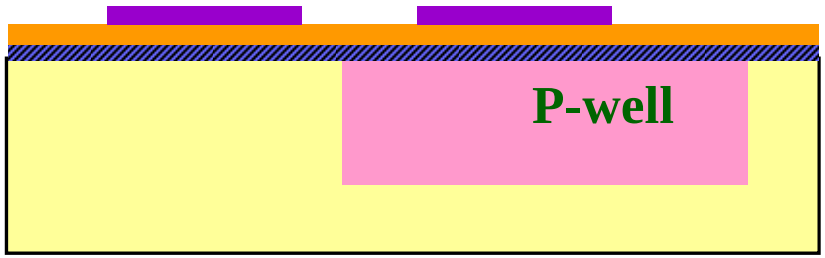
氮化膜生长

2. 光刻有源区：

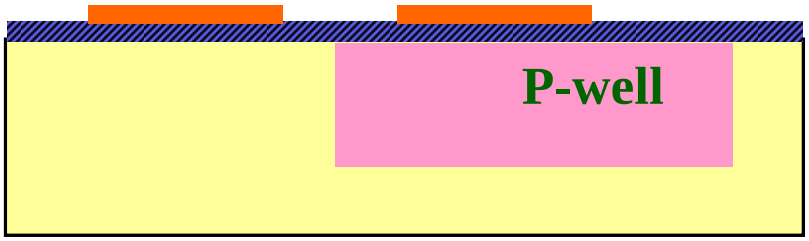


涂胶

对版曝光

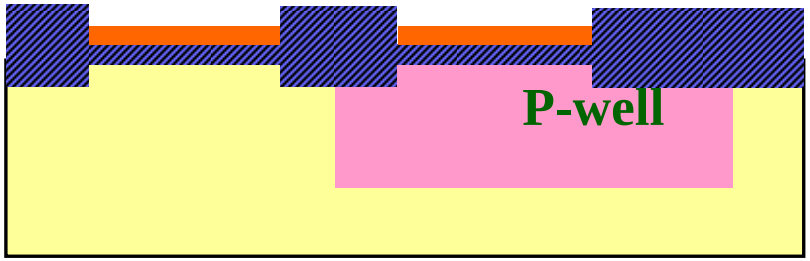


显影

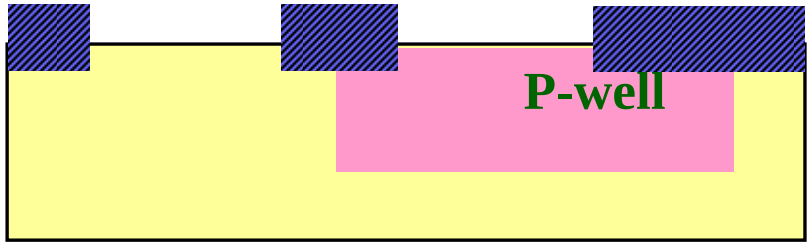


氮化硅刻蚀去胶

3. 场区氧化：

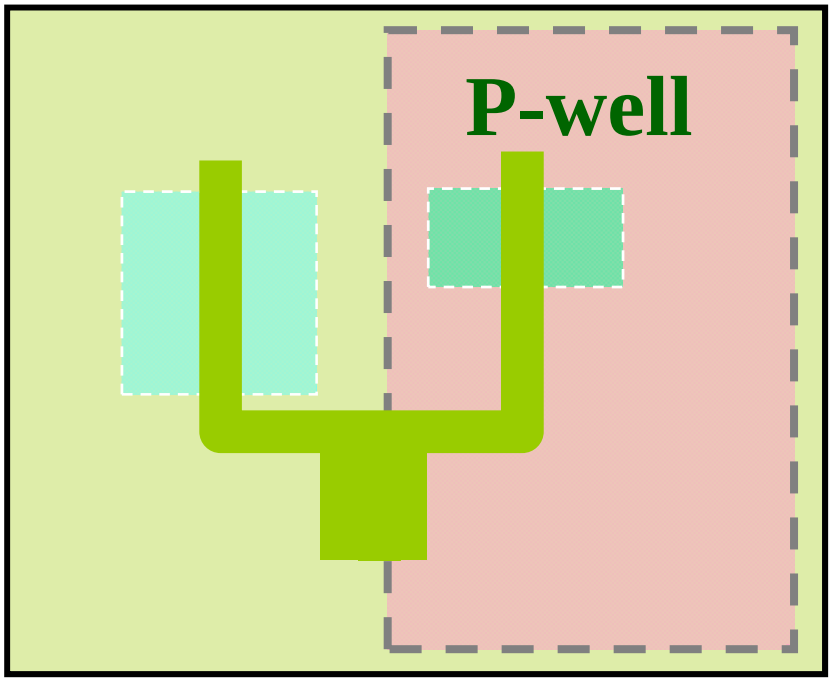


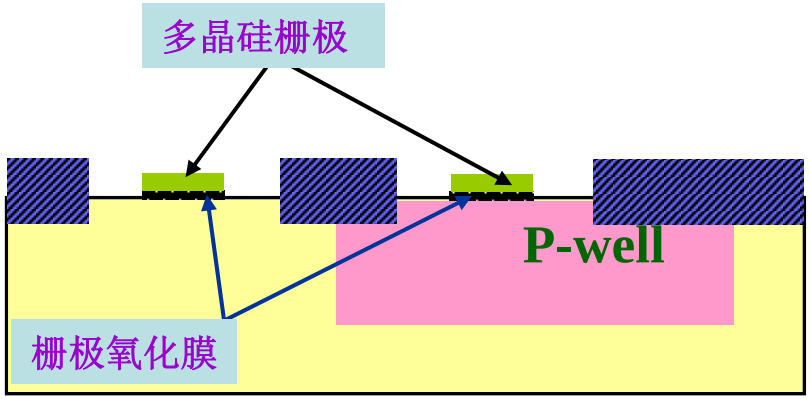
场区氧化（湿法氧化）



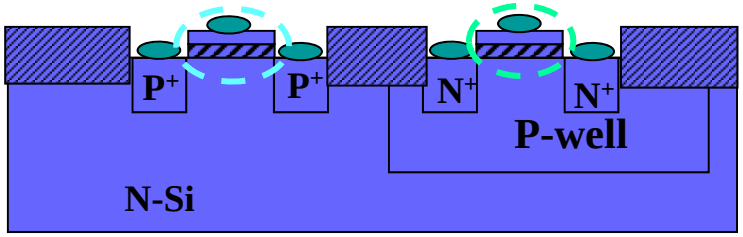
去除氮化硅薄膜及有源区SiO_2

掩膜3：　光刻多晶硅

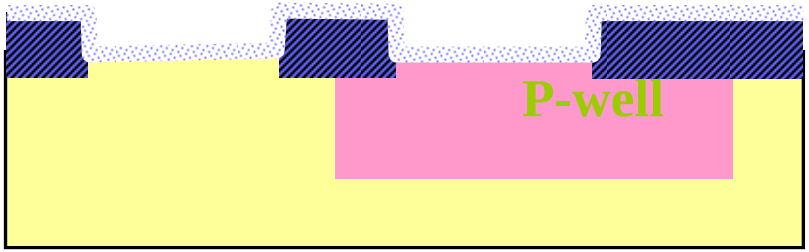




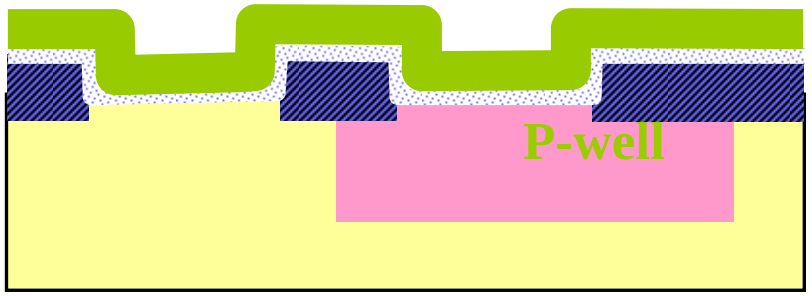
去除氮化硅薄膜及有源区SiO_2



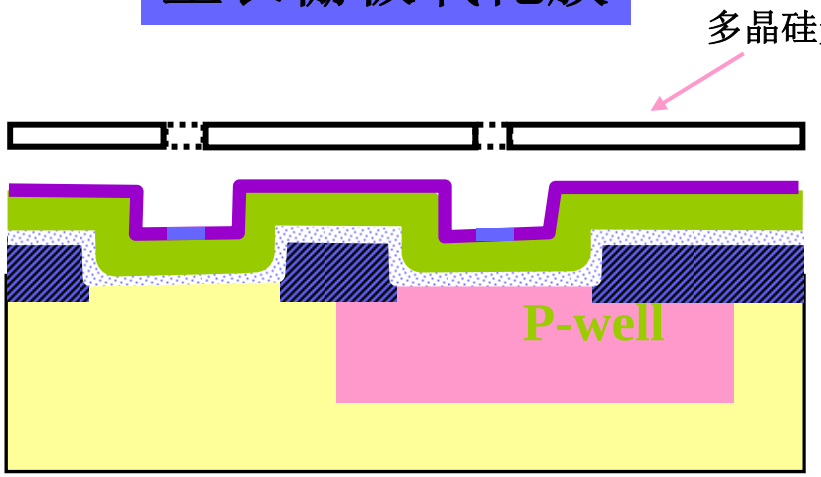
- 生长栅极氧化膜
- 淀积多晶硅
- 光刻多晶硅



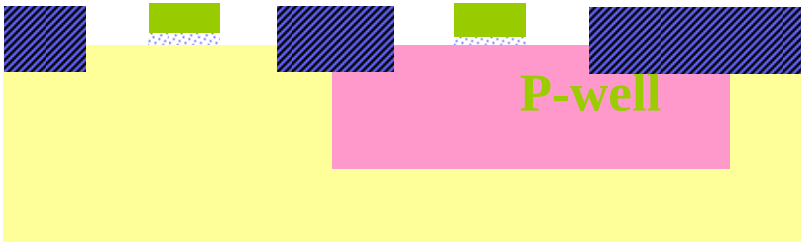
生长栅极氧化膜



淀积多晶硅

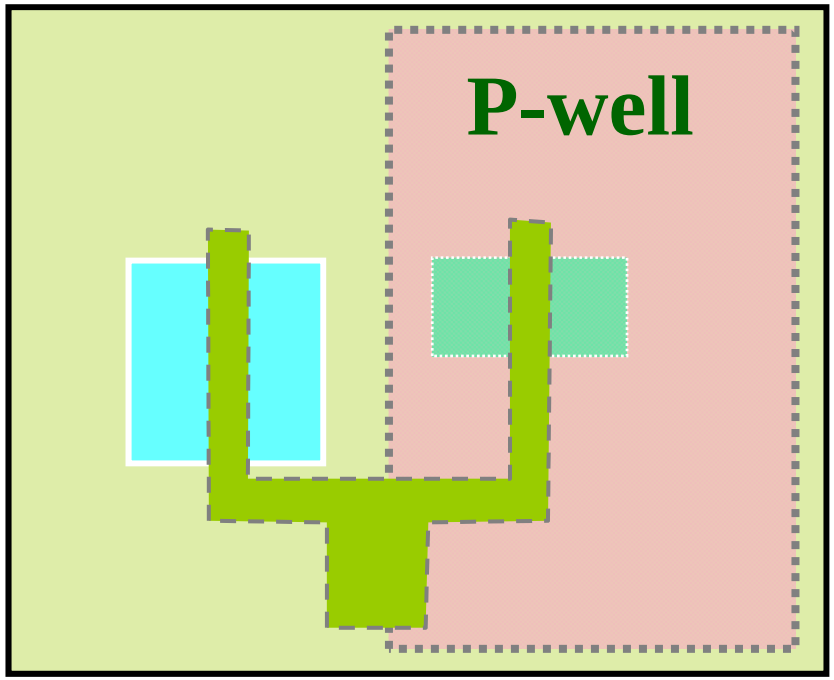


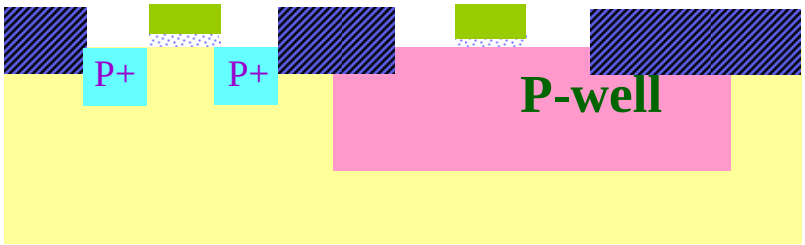
涂胶光刻

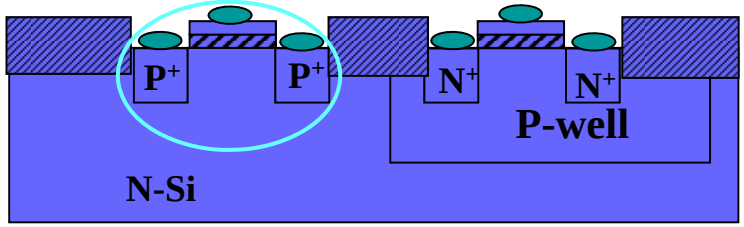


多晶硅刻蚀

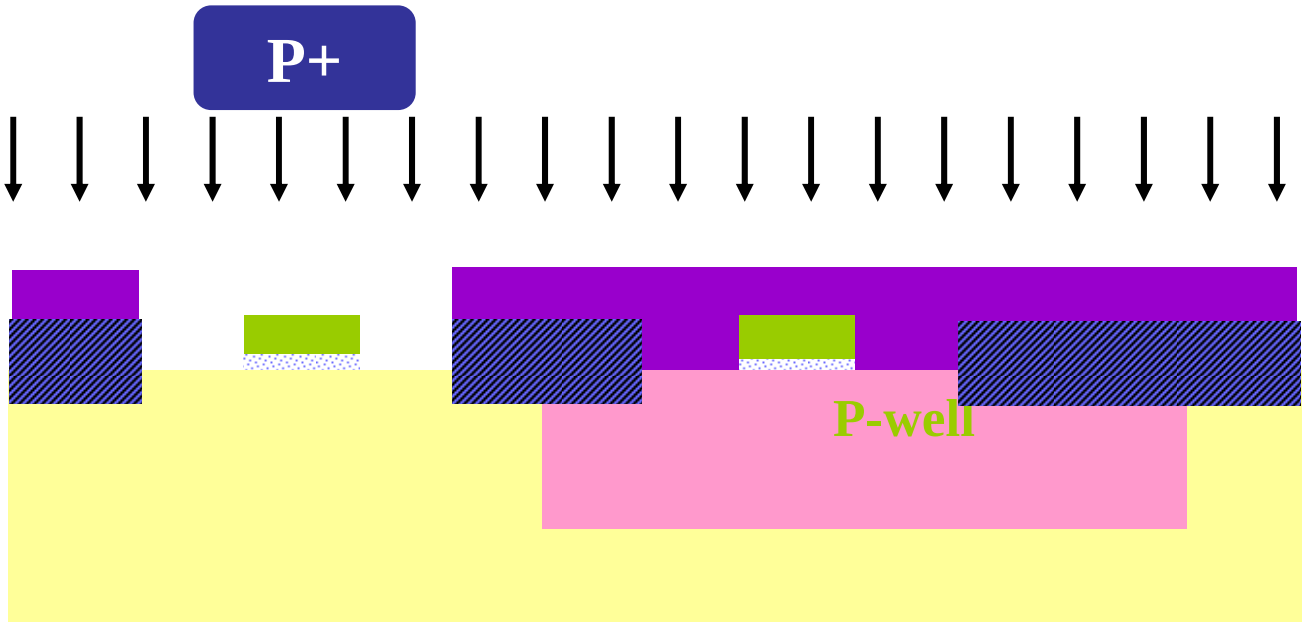
掩膜4 ： P+区光刻



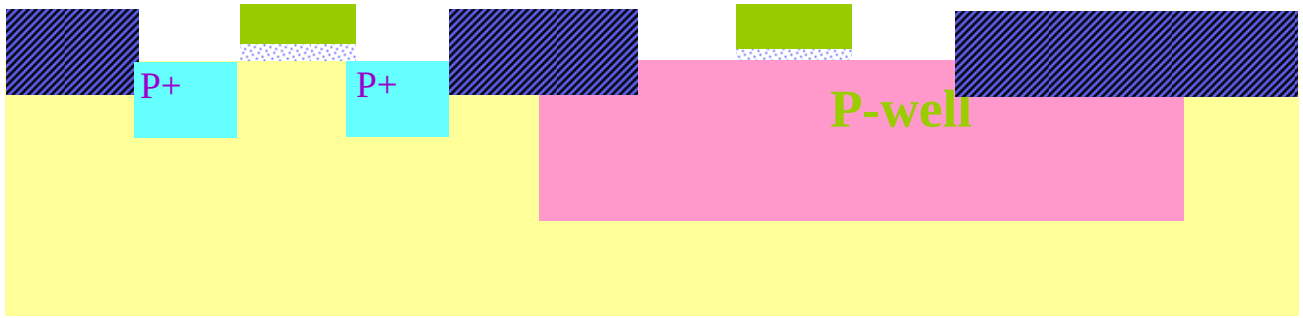




1、P+区光刻
2、离子注入B+，栅区有多晶硅做掩蔽，称为硅栅自对准工艺。
3、去胶

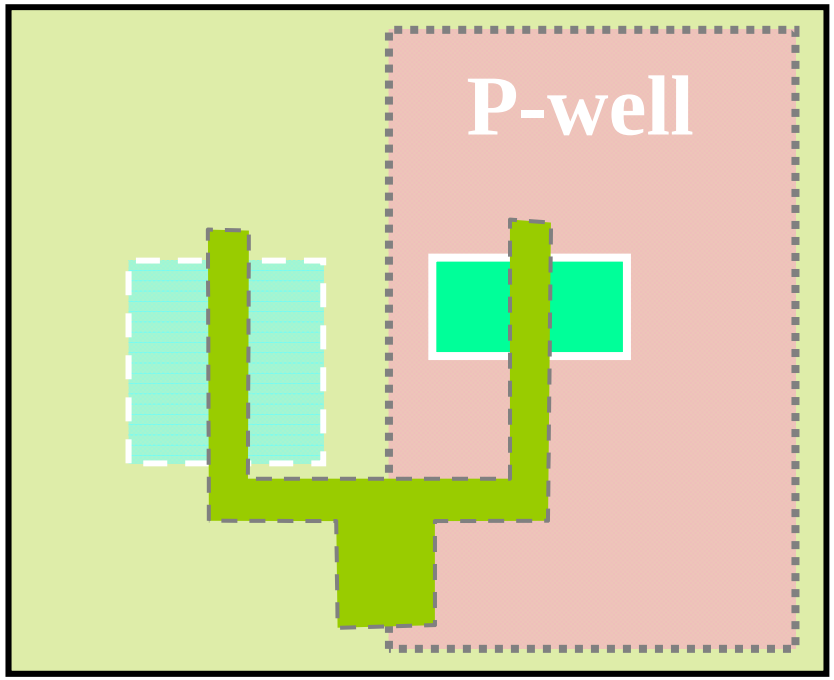


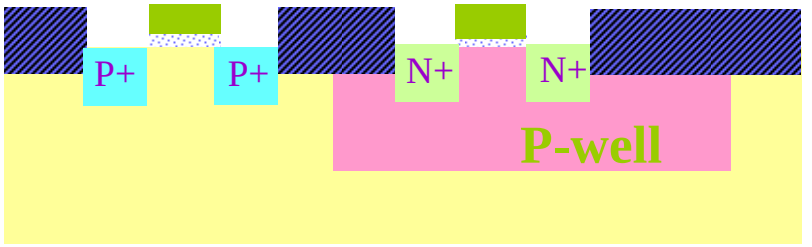
硼离子注入

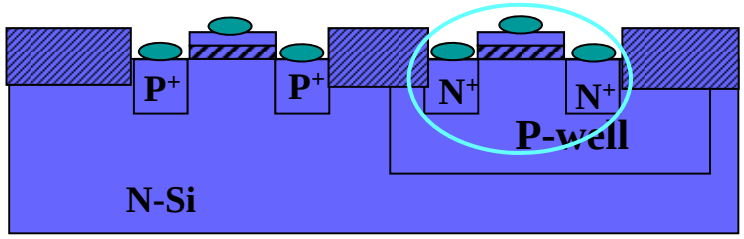


去胶

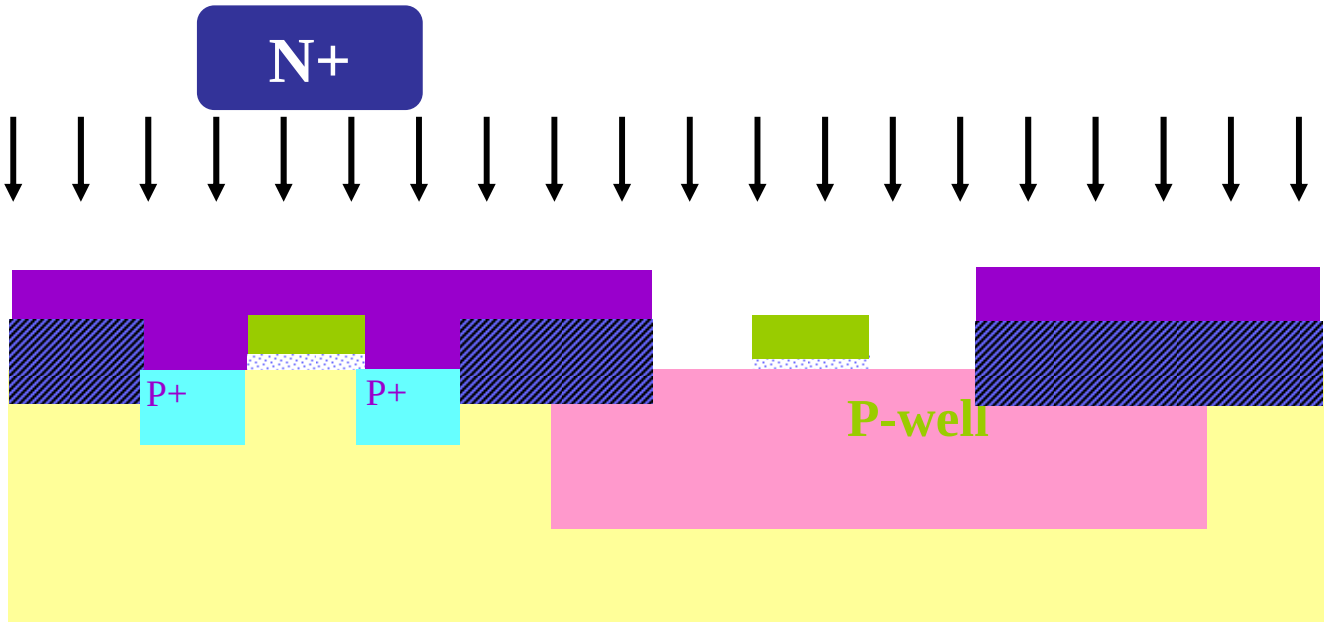
掩膜5 ： N+区光刻



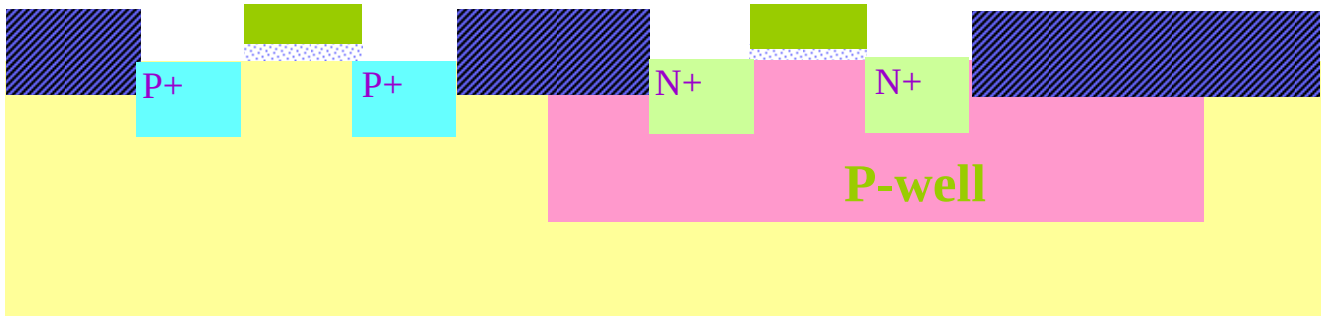




1、N+区光刻
2、离子注入P+，栅区有多晶硅做掩蔽，称为硅栅自对准工艺。
3、去胶

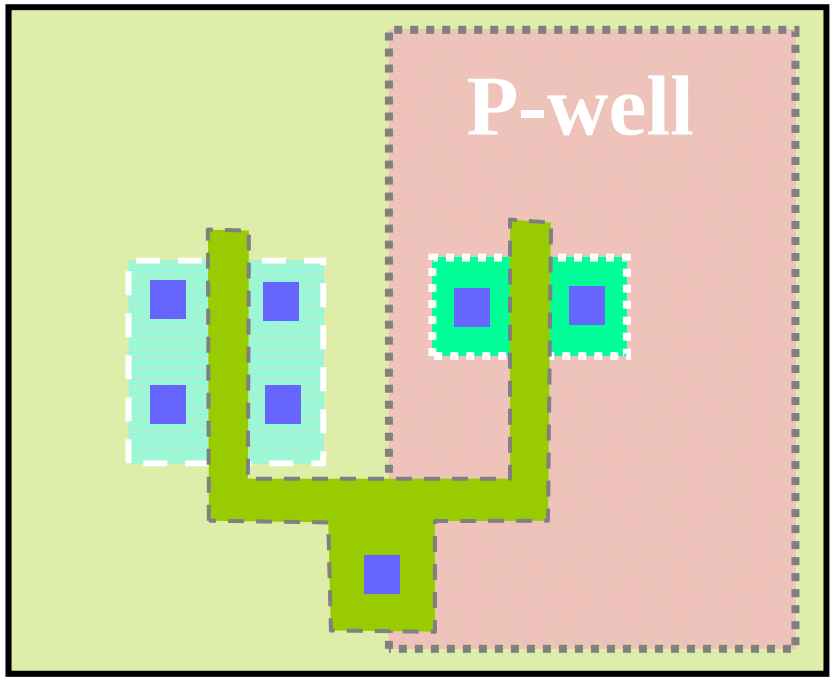


磷离子注入

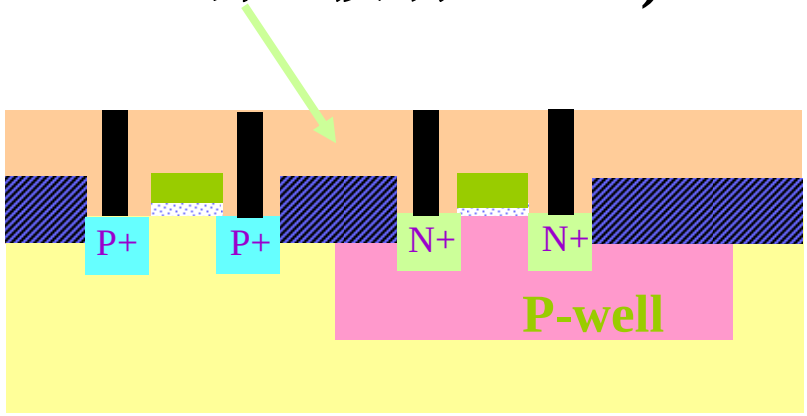


去胶

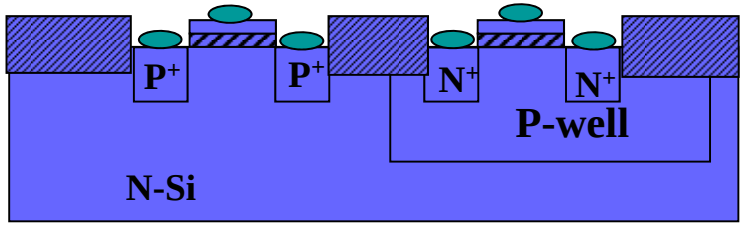
掩膜6 ： 光刻接触孔



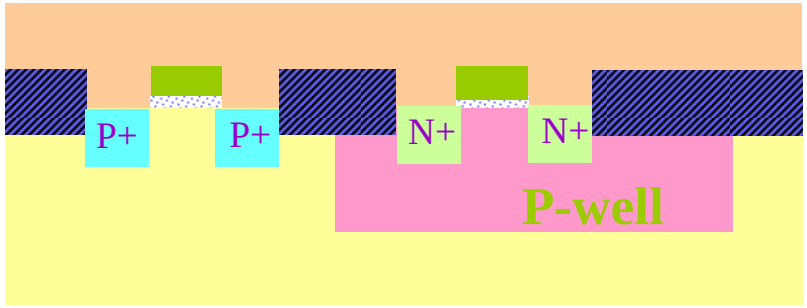
磷硅玻璃（PSG)



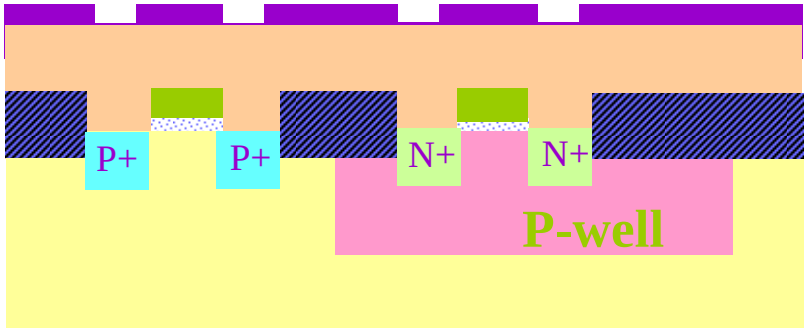
1、淀积PSG.
2、光刻接触孔
3、刻蚀接触孔



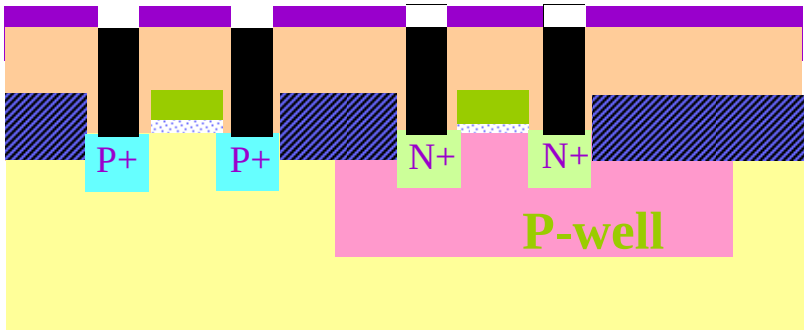
掩膜6 ： 光刻接触孔



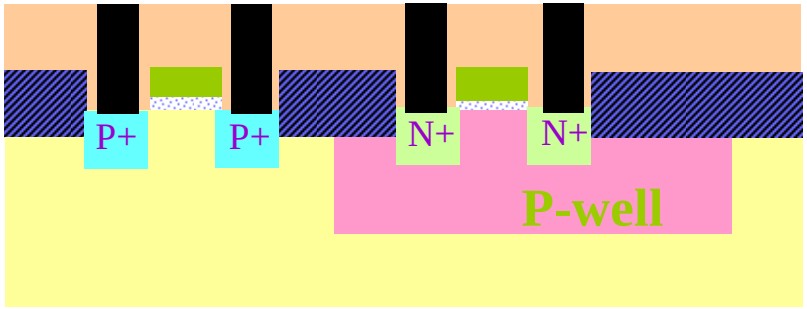
淀积PSG



光刻接触孔



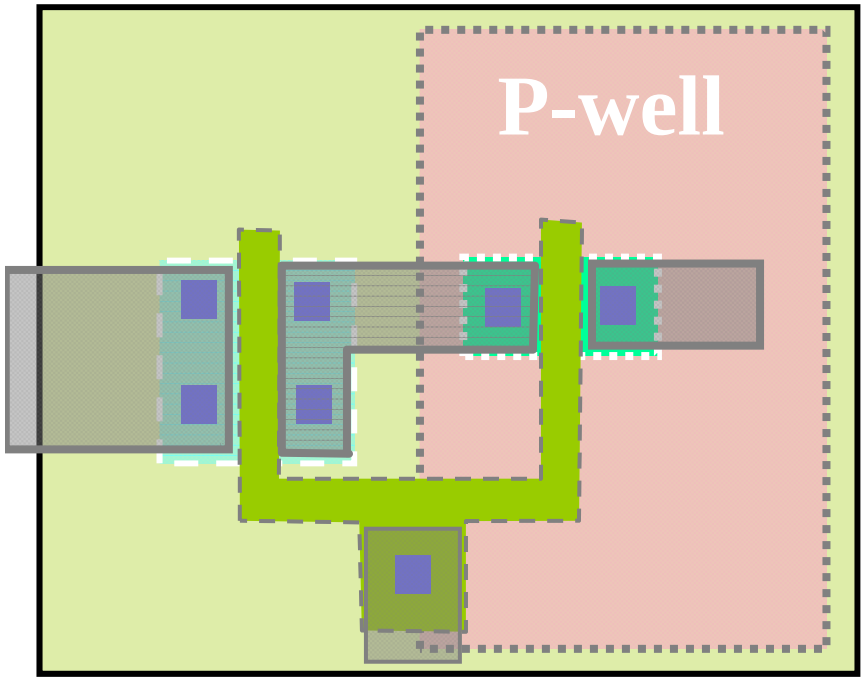
刻蚀接触孔

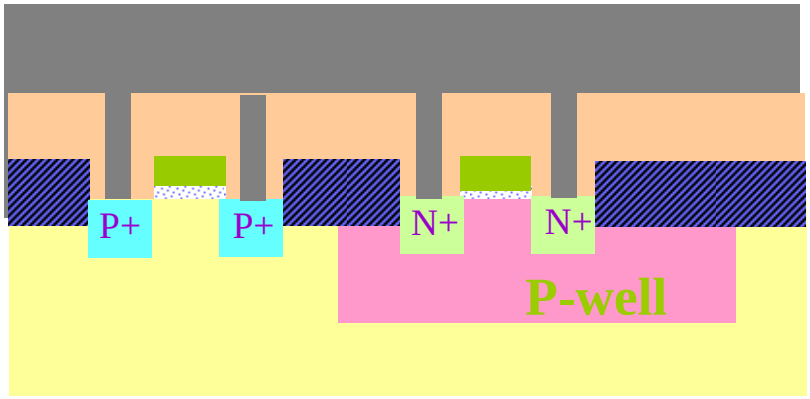


去胶

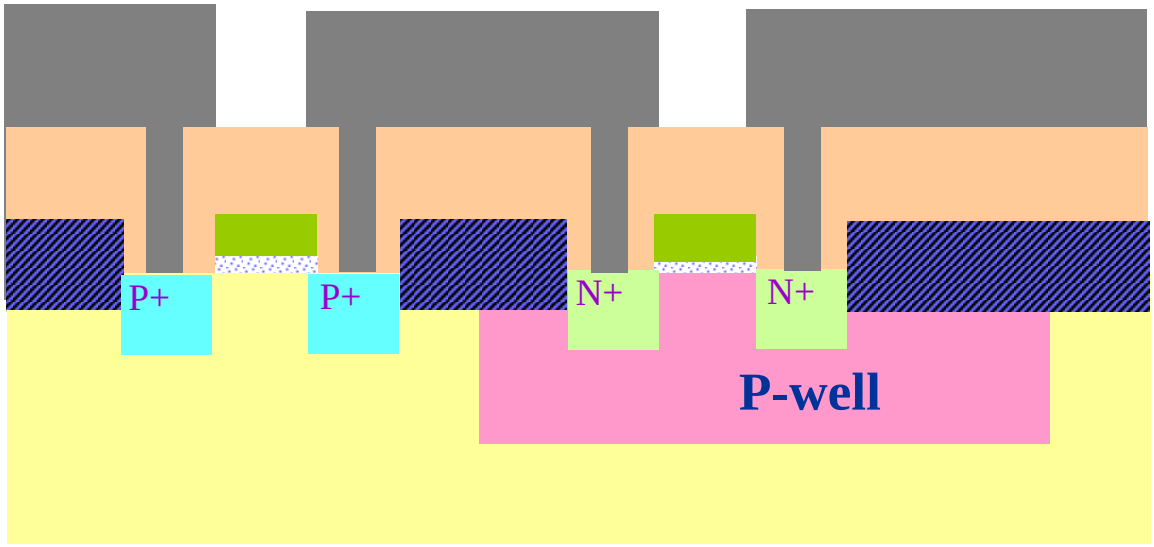
●CVD装置内部

掩膜7 ： 光刻铝线





1、淀积铝.
2、光刻铝
3、去胶



铝线

PSG

场氧

栅极氧化膜

N+区

P+区

P-well

N-型硅极板

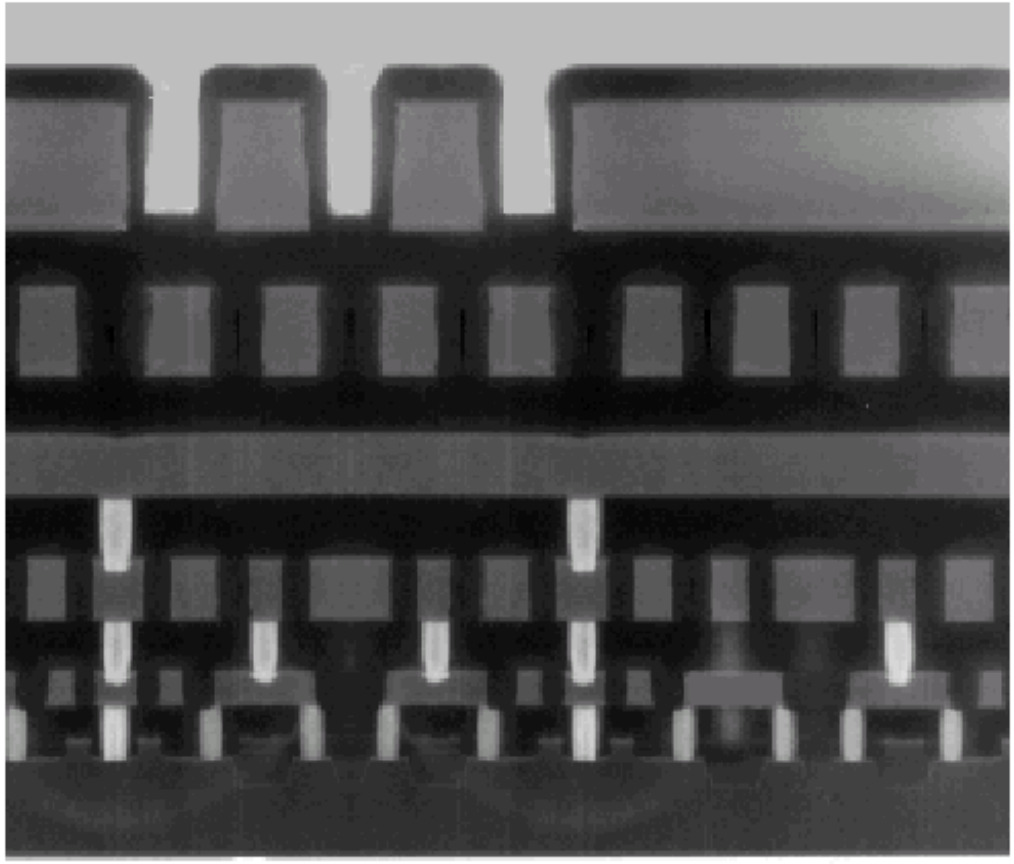
多晶硅

Example: Intel 0.25 micron Process

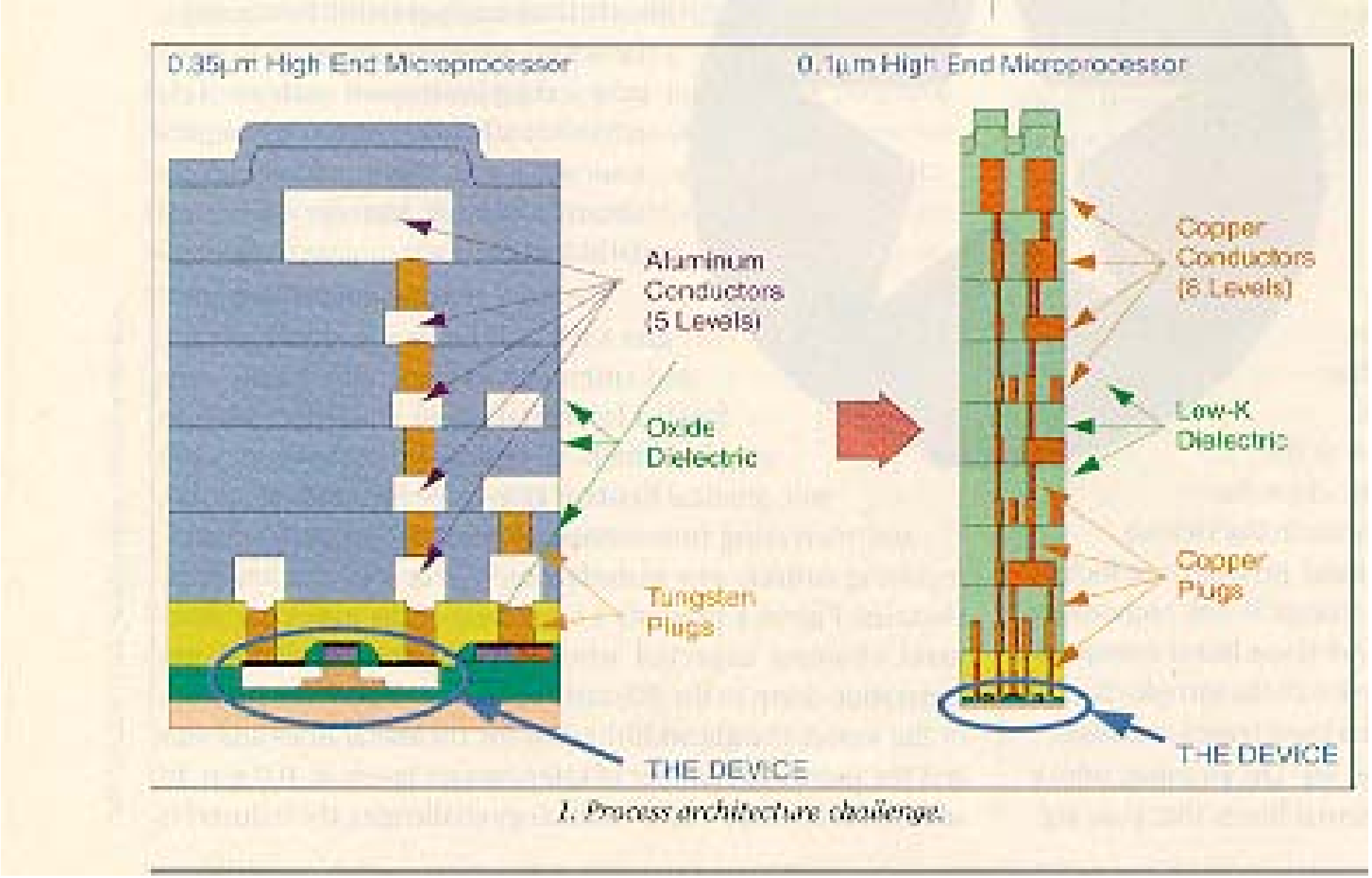
5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio

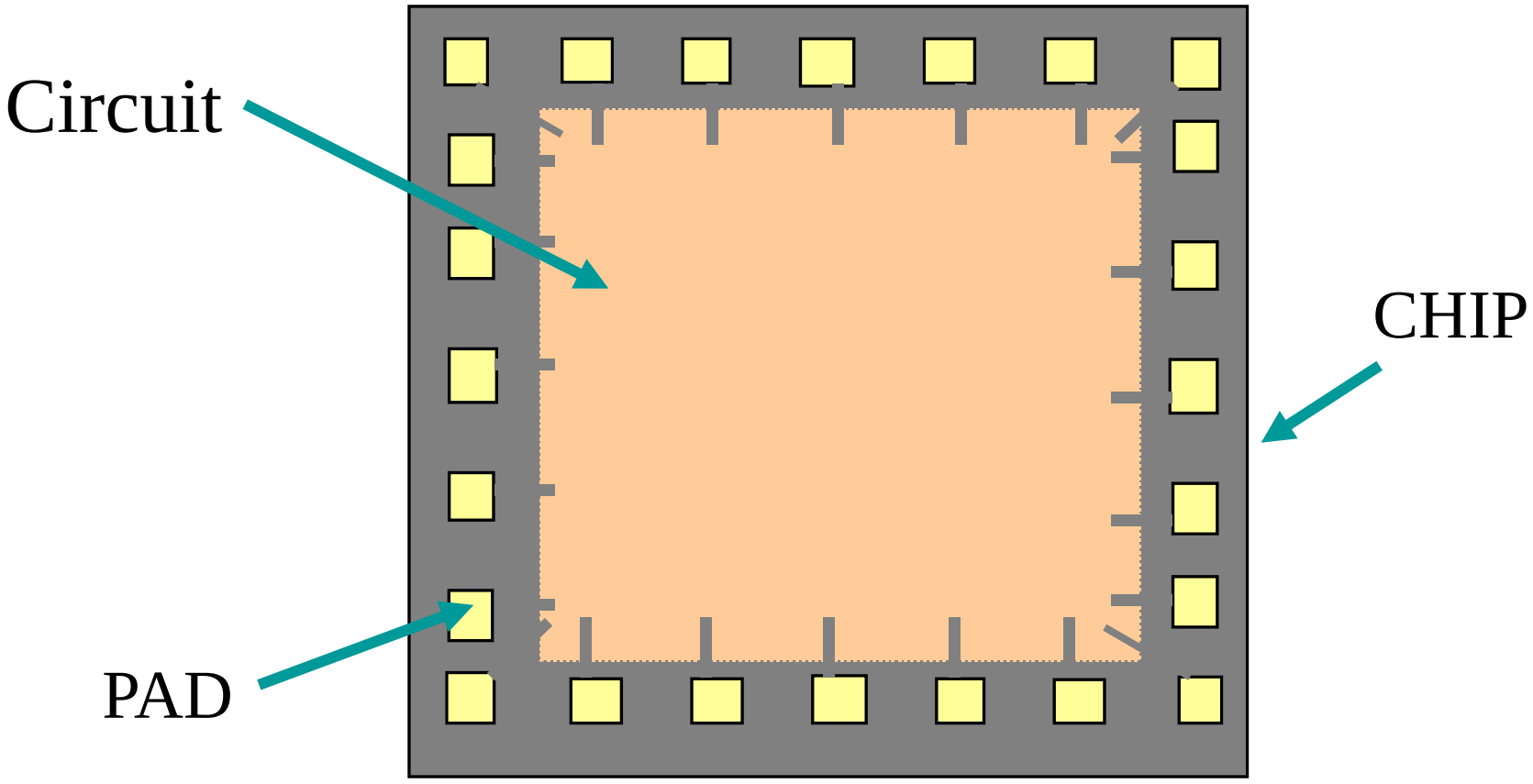


Interconnect Impact on Chip

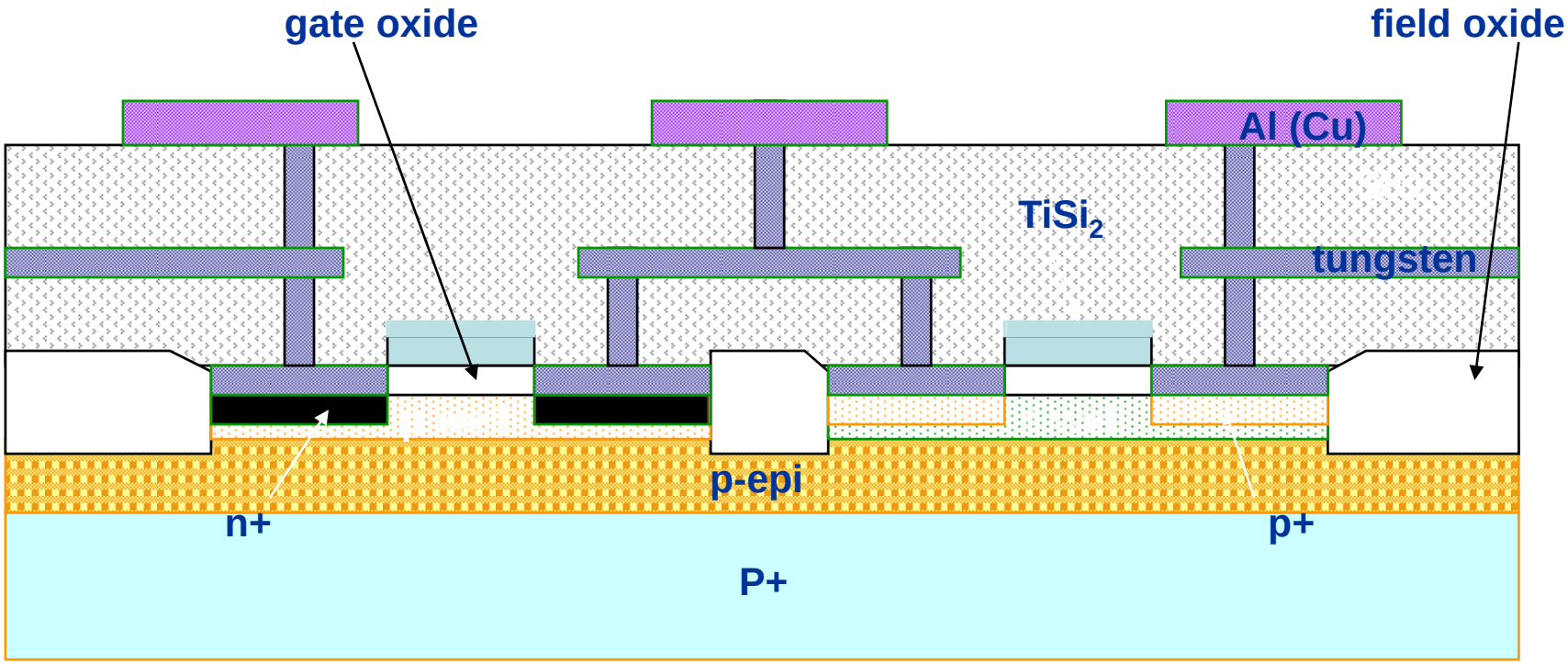


1. Process architecture challenge.

掩膜8：刻钝化孔



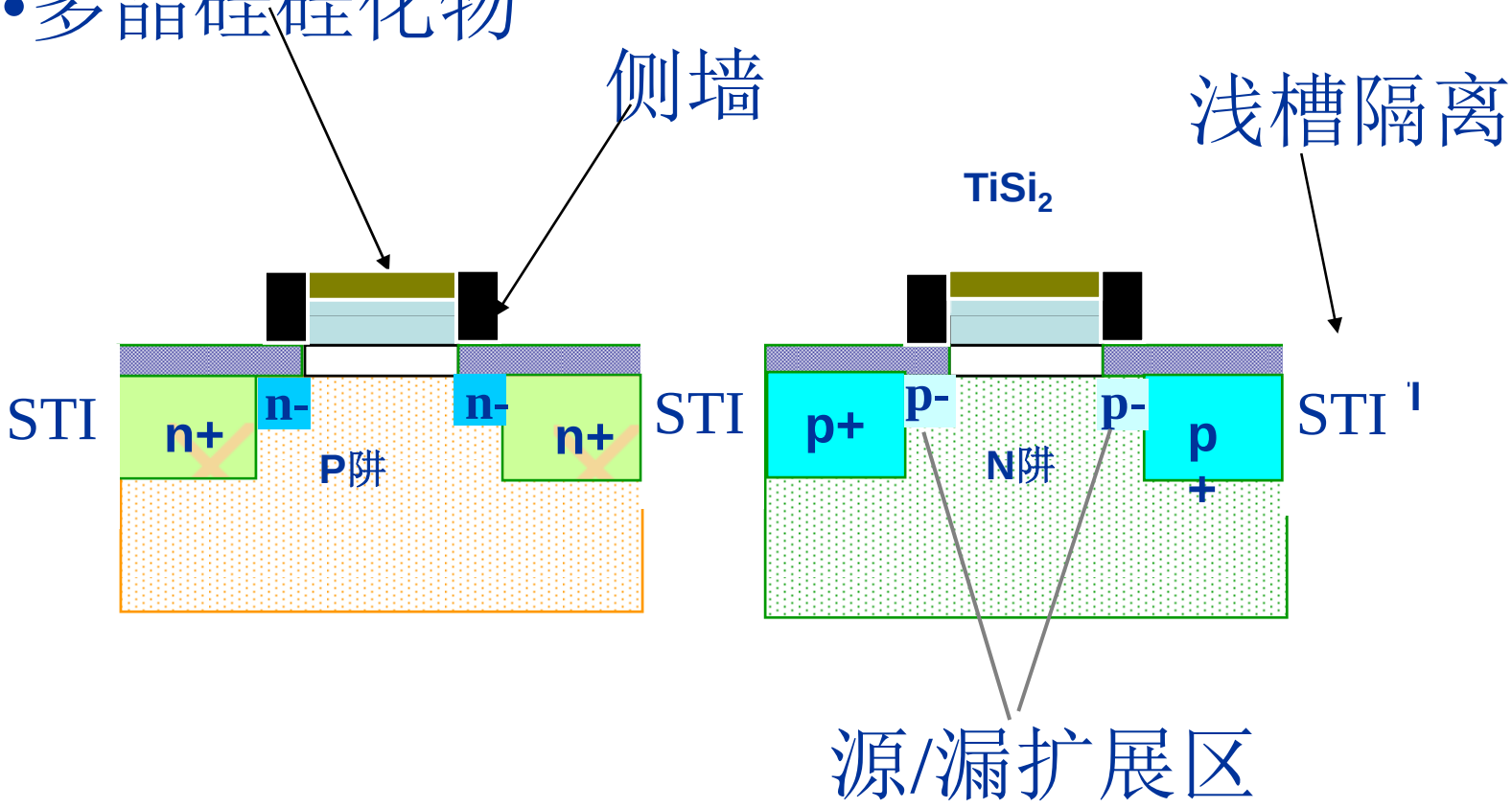
双阱标准CMOS工艺



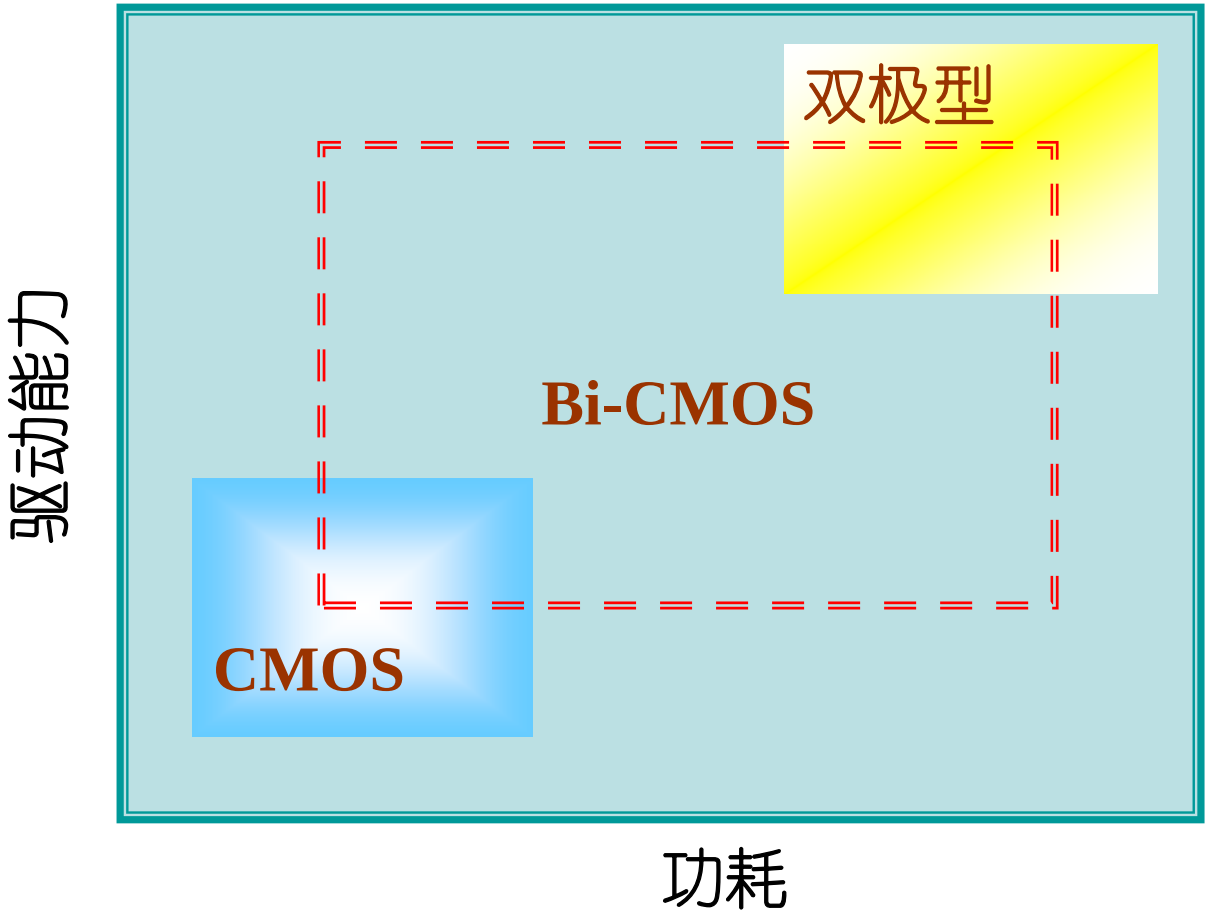
- 增加器件密度
- 防止寄生晶体管效应（闩锁效应）

深亚微米CMOS晶体管结构

- 多晶硅硅化物



BiCMOS集成电路工艺

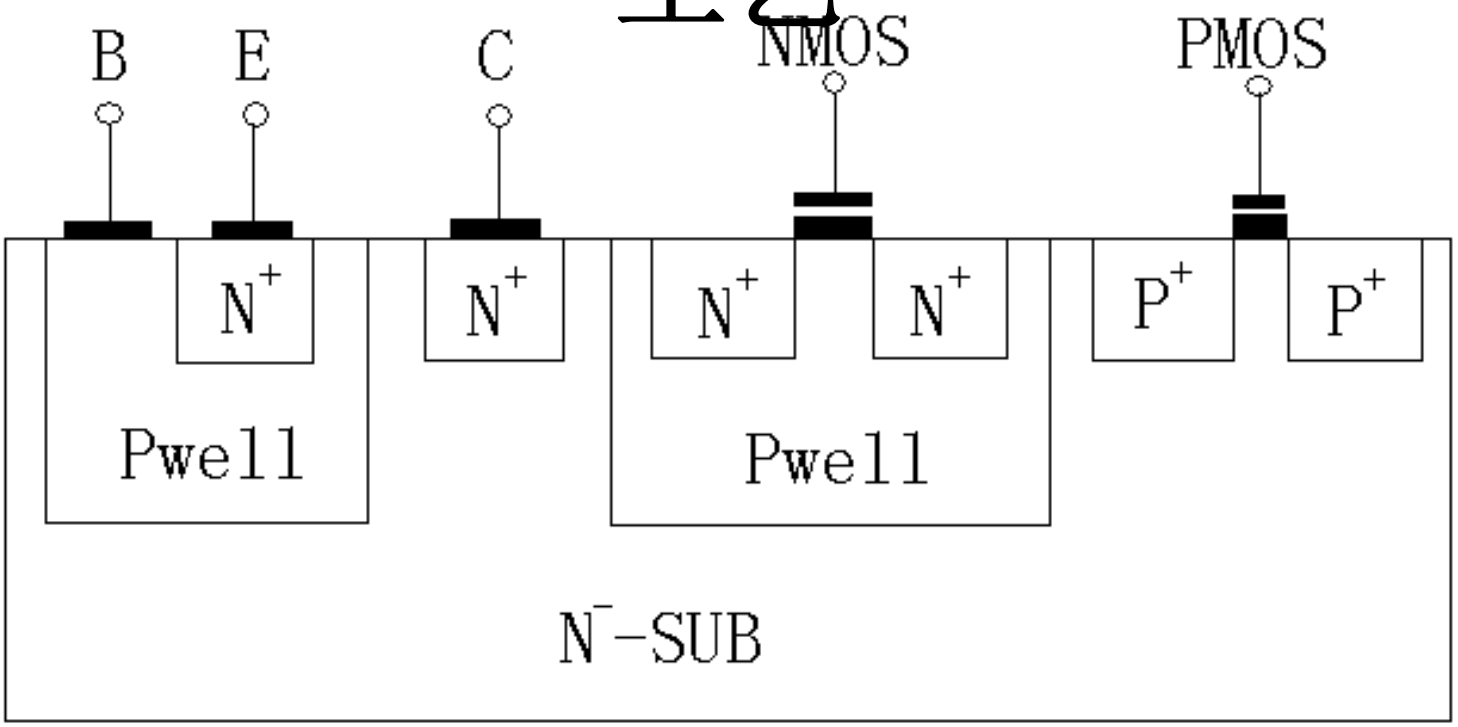


BiCMOS工艺分类

- 以CMOS工艺为基础的BiCMOS工艺

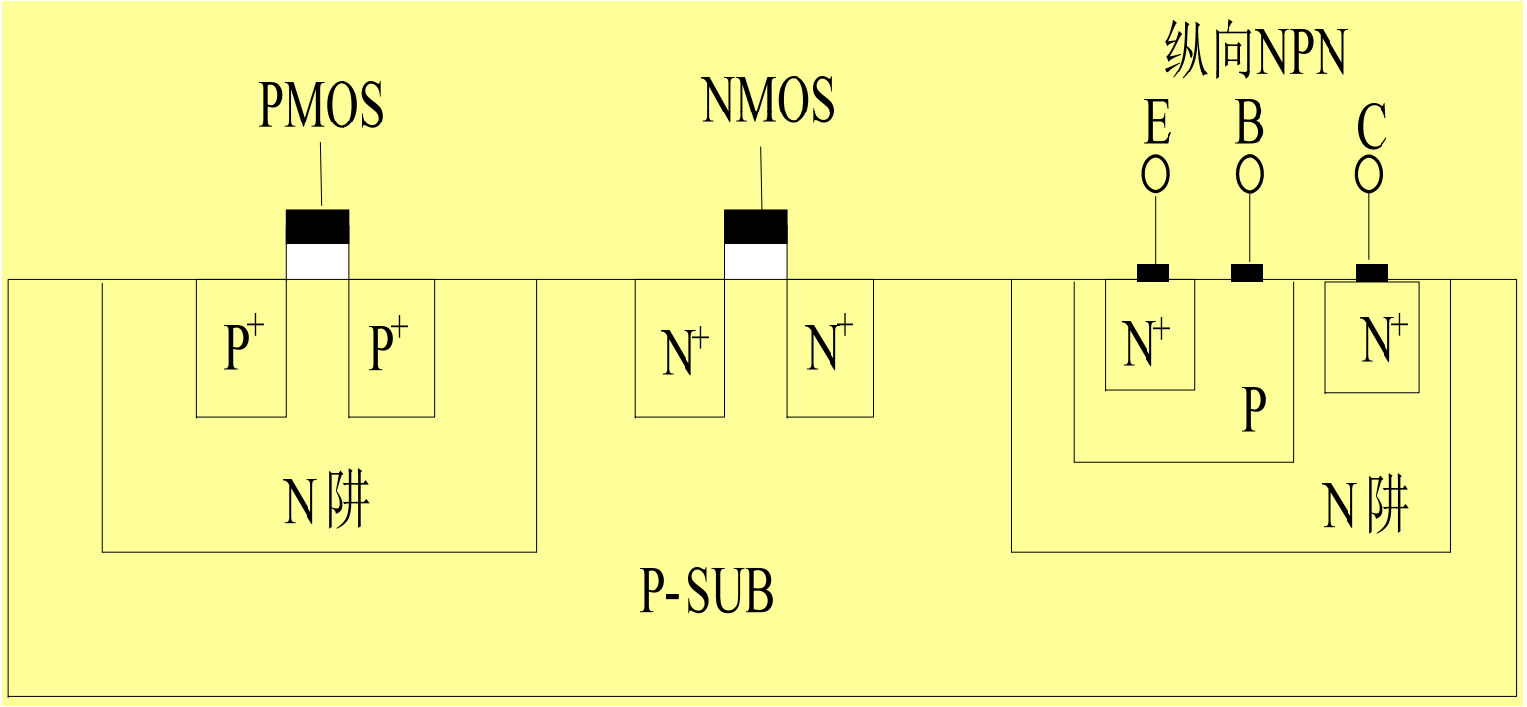
- 以双极工艺为基础的BiCMOS工艺。

以P阱CMOS工艺为基础的BiCMOS工艺



- NPN晶体管电流增益小；
- 集电极的串联电阻很大;
- NPN管C极只能接固定电位，从而限制了NPN管的使用

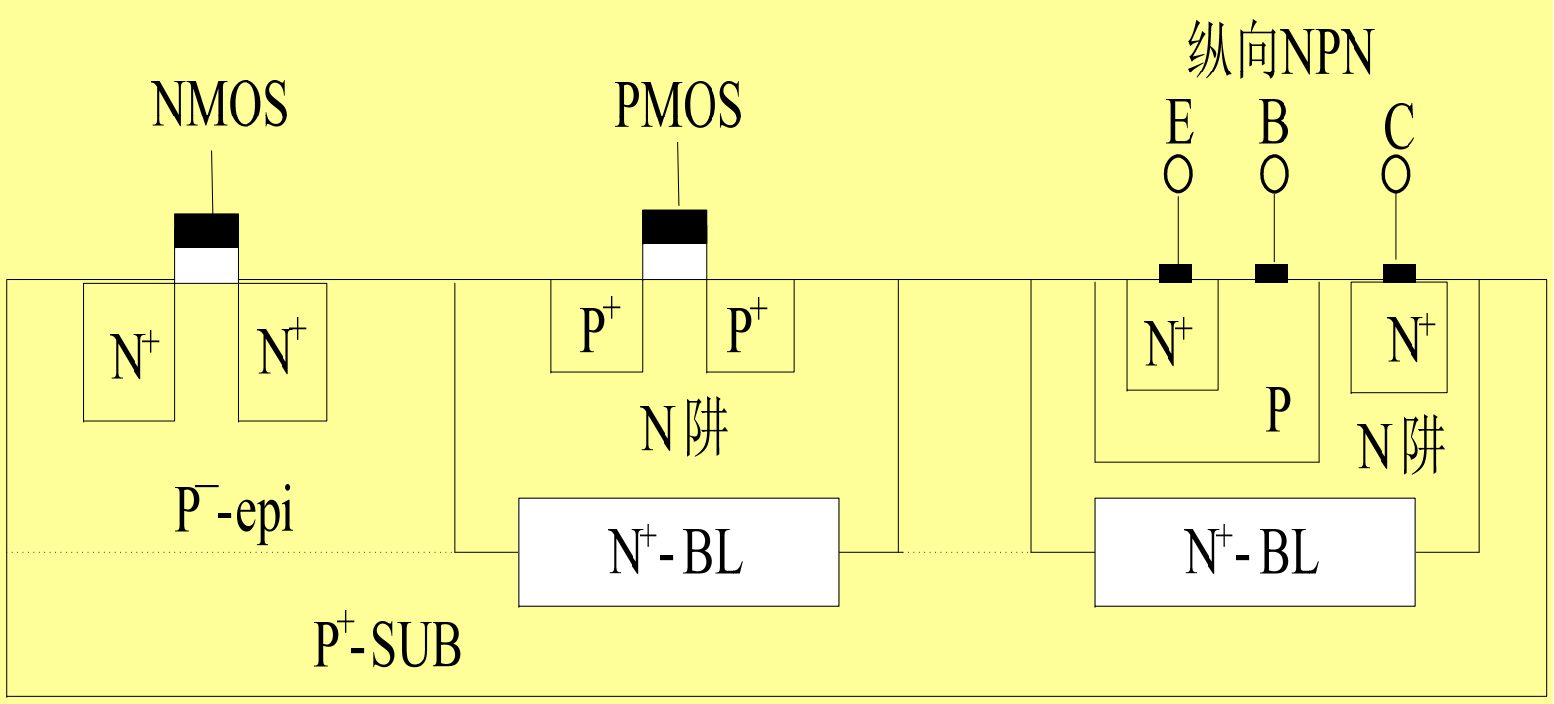
以N阱CMOS工艺为基础的BiCMOS工艺



- NPN具有较薄的基区，提高了其性能；
- N阱使得NPN管C极与衬底隔开，可根据电路需要接电位
- 集电极串联电阻还是太大，影响双极器件的驱动能力

在现有N阱CMOS工艺上增加一块掩膜板

以N阱CMOS工艺为基础的改进BiCMOS工艺



- 使NPN管的集电极串联电阻减小5~6倍；
- 使CMOS器件的抗闩锁性能大大提高

三、后部封装 （在另外厂房）

（1）背面减薄

（2）切片

（3）粘片

（4）压焊：金丝球焊

（5）切筋

（6）整形

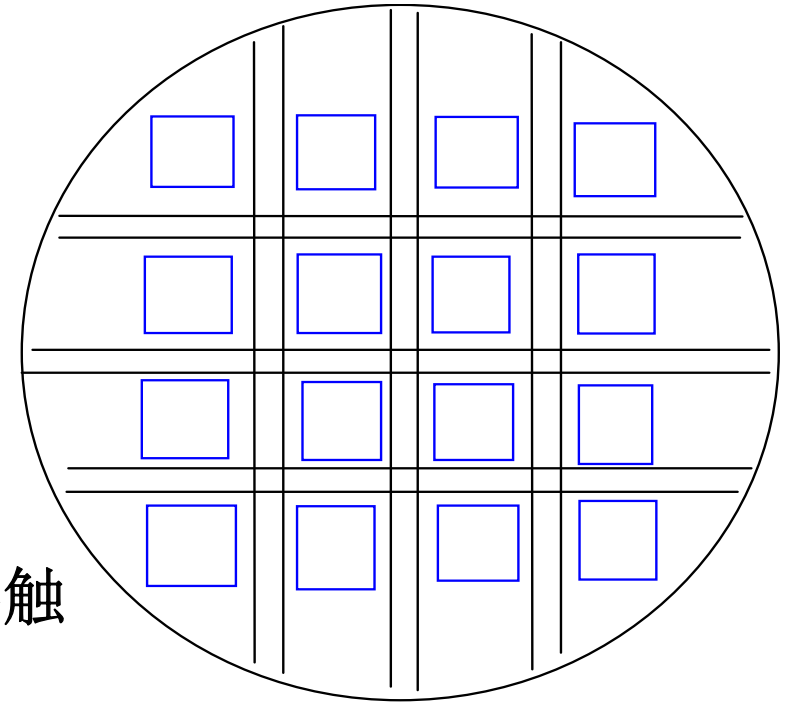
（7）所封

（8）沾锡：保证管脚的电学接触

（9）老化

（10）成测

（11）打印、包装



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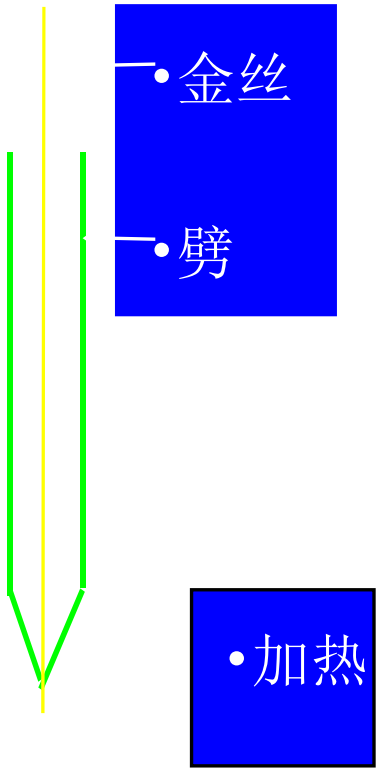
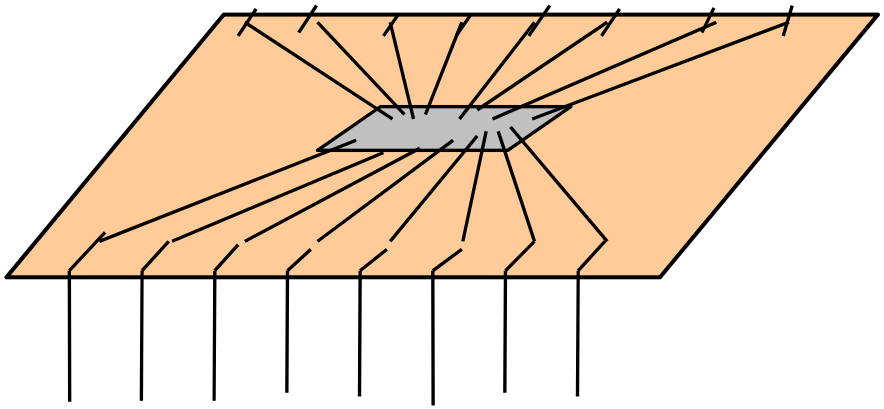
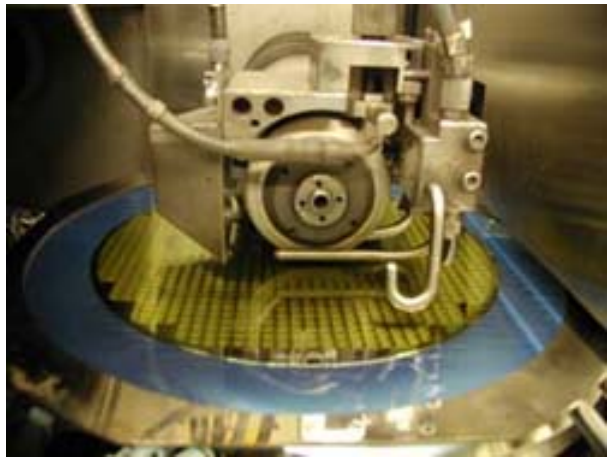
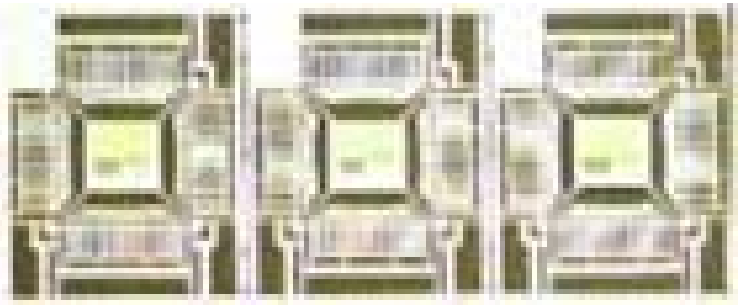


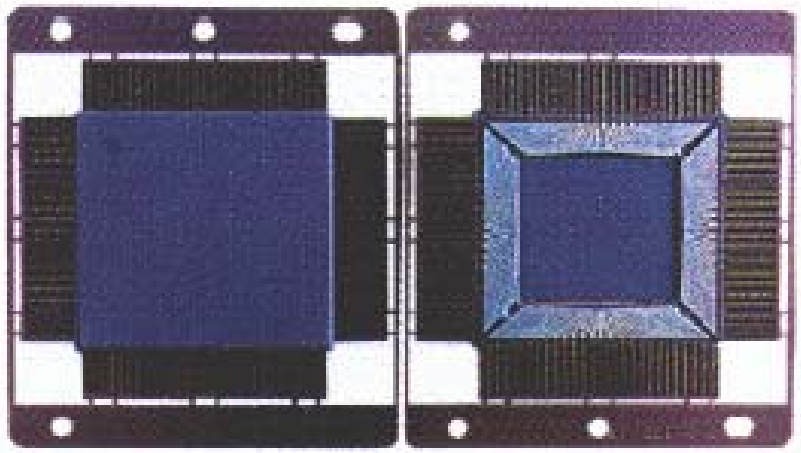


压　　焊

三、后部封装 （在另外厂房）







208-lead AlN quad flat package