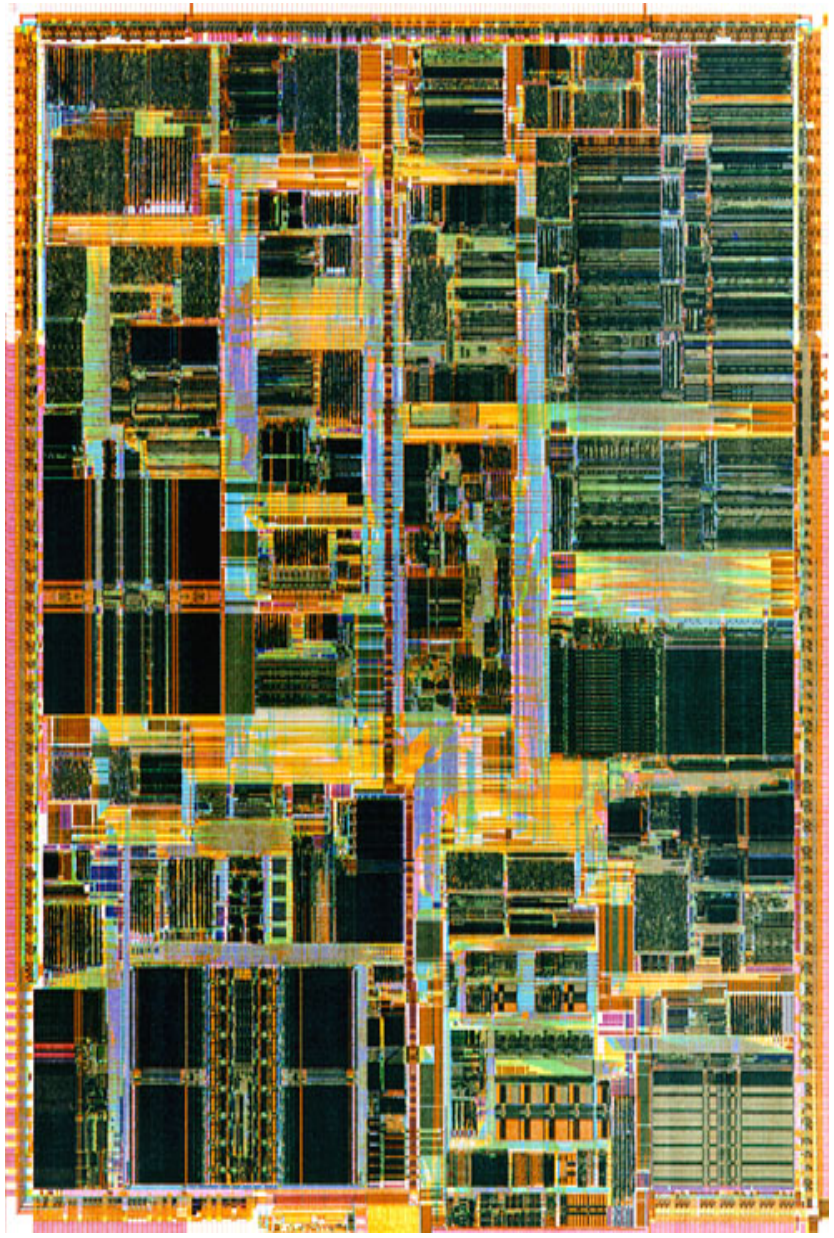


半导体集成电路

学校：西安理工大学

院系：自动化学院电子工程系

专业：电子、微电

时间：秋季学期

上一节课要点

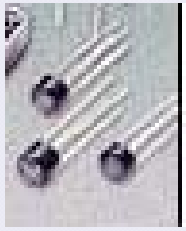
1. 集成电路的基本概念
2. 半导体集成电路的分类
3. 半导体集成电路的几个重要概念

内容概述

集成电路

- 按器件类型分
  - 双极型集成电路
    - TTL、ECL
    - I^2L等
  - BiCMOS集成电路
  - MOS集成电路
    - PMOS
    - NMOS
    - CMOS
- 按集成度分
  - SSI（100以下个等效门）
  - MSI（<10^3个等效门）
  - LSI （<10^4个等效门）
  - VLSI（>10^4个以上等效门）
- 按信号类型分
  - 模拟集成电路
  - 数模混合集成电路
  - 数字集成电路

集成度、工作频率、电源电压、特征尺寸、硅片直径

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第2章

双极集成电路中的元件形成及其寄生效应

第2章 内容提要

2.1 双极集成电路制造工艺

2.1.1 双极型晶体管的单管结构和工作原理

2.1.2双极集成晶体管的结构与制造工艺

2.2 理想本征双极晶体管的埃伯斯-莫尔(EM)模型

2.2.1 一结两层二极管的EM模型

2.2.2 两结三层三极管的EM模型

2.2.3 三结四层三极管的EM模型

2.3 集成双极晶体管的有源寄生

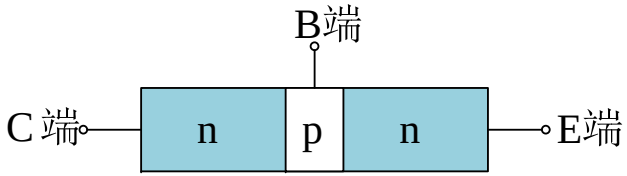
本节课内容

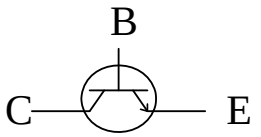
2.1.1 双极型晶体管的单管结构和工作原理

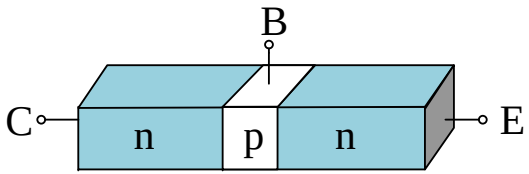
2.1.2 双极集成晶体管的结构与制造工艺

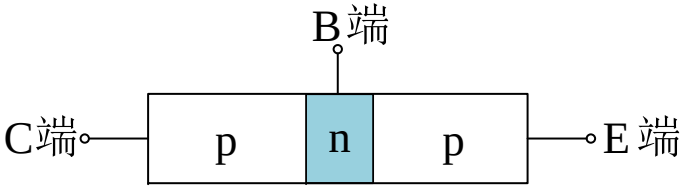
2.1.1 双极晶体管的单管结构及工作原理

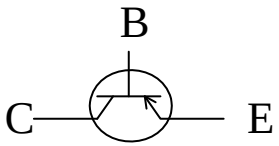
- 双极器件：两种载流子（电子和空穴）同时参与导电

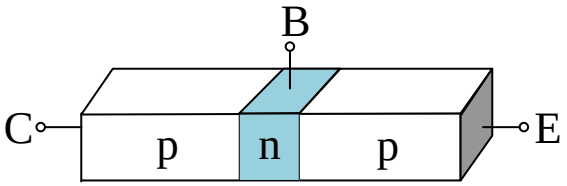




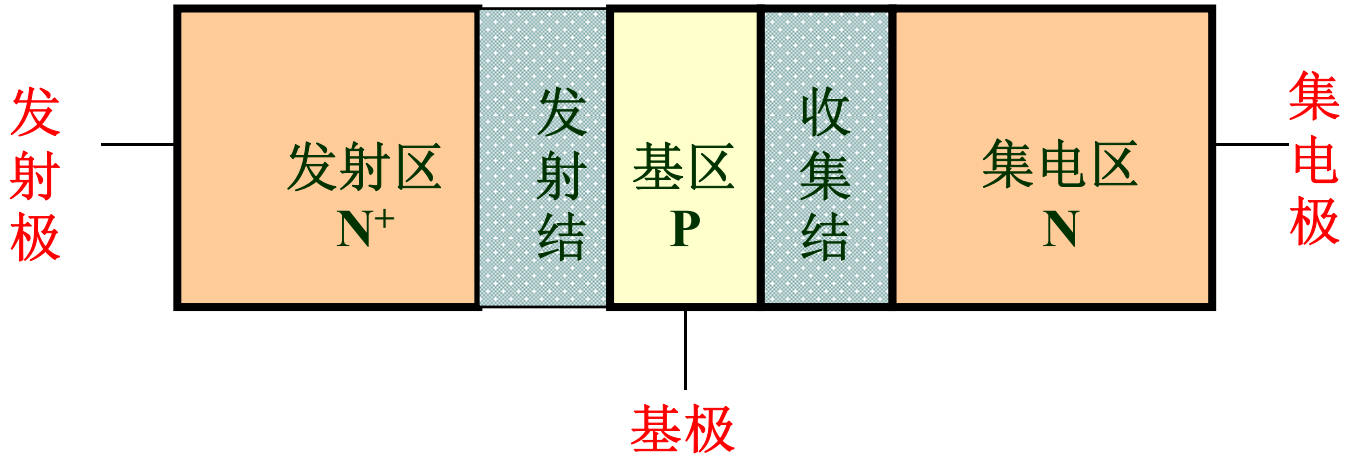


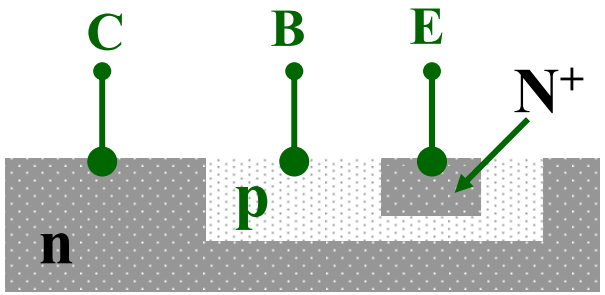






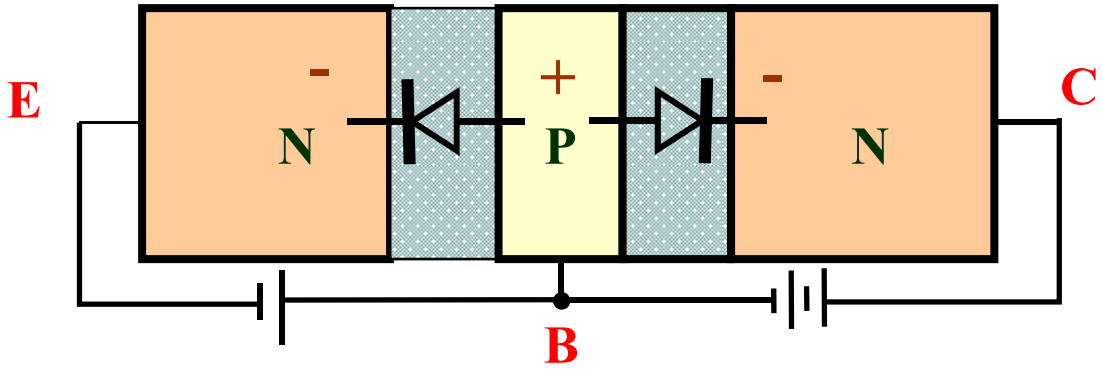
◆ npn双极晶体管单管结构示意图



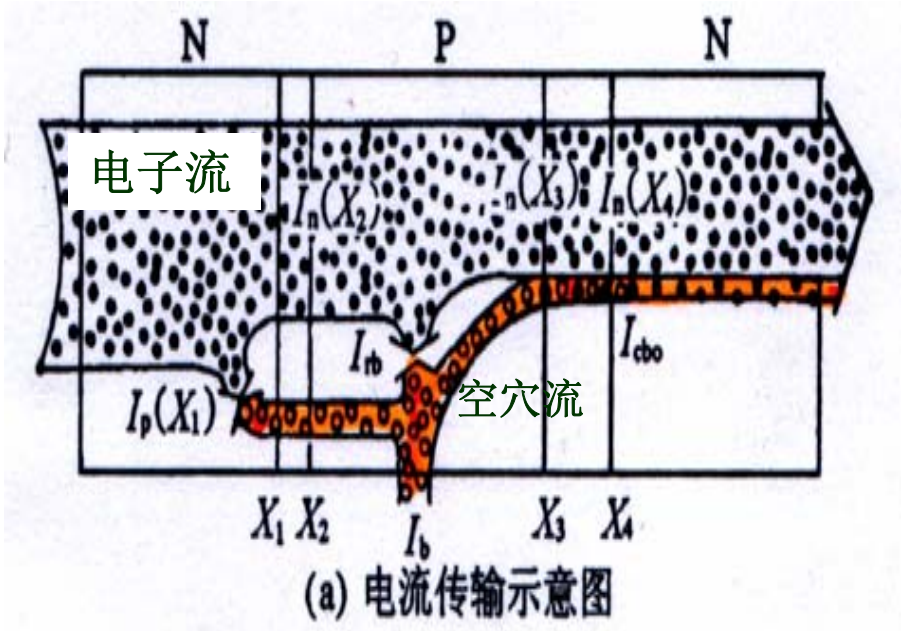


结构特点

1. 发射区掺杂浓度最大
2. 基区次之、集电极掺杂最小
3. 基区宽度很窄

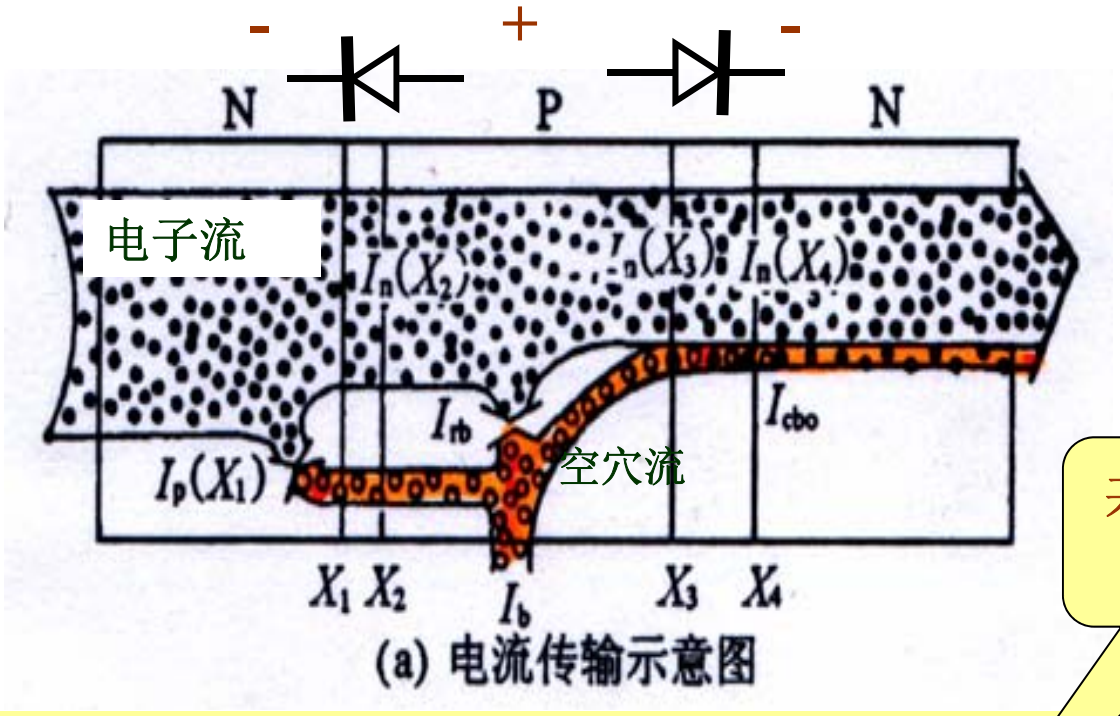


当发射结正偏（V_{BE}>0)，集电结反偏（V_{BC}<0)时，为正向工作区。



(a) 电流传输示意图

$I_e = I_p(X_1) + I_n(X_2)$　$I_b = I_p(X_1) + I_{rb} - I_{cbo}$　$I_c = I_n(X_4) + I_{cbo}$



(a) 电流传输示意图

共基极短路电流增益

正向工作区

- 发射结正偏，发射极发射电子，在基区中扩散前进，大部分被集电极反偏结收集：$I_c = \alpha I_e + I_{cbo} \approx \alpha I_e$（α 接近于1）

$$\boldsymbol{I_e = I_c + I_b} \quad I_e - I_c = I_b \quad I_c - \alpha I_c = \alpha I_b \quad \therefore I_c = \frac{\alpha}{1-\alpha} I_b \quad \text{令 } \beta = \frac{\alpha}{1-\alpha}$$

- 具有电流放大作用：$I_c \approx \beta I_b$

共射极短路电流增益

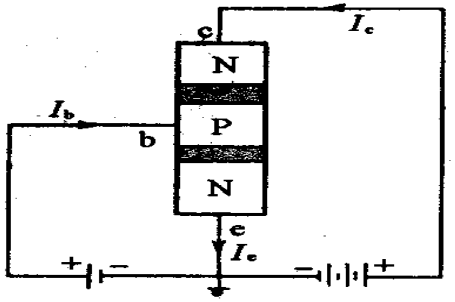
◆ 共发射极的直流特性曲线

三个区域：

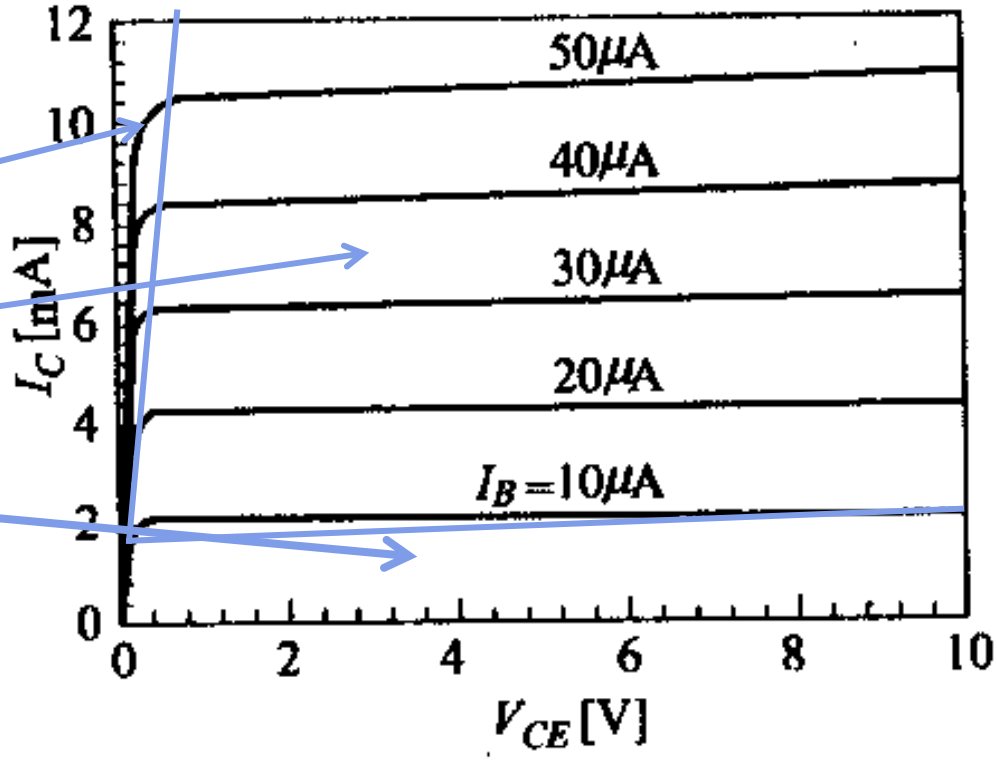
饱和区

放大区

截止区



晶体管的共发射极接法



(b) 发射极接地特性

2.1.2 双极晶体管的结构及制作工艺

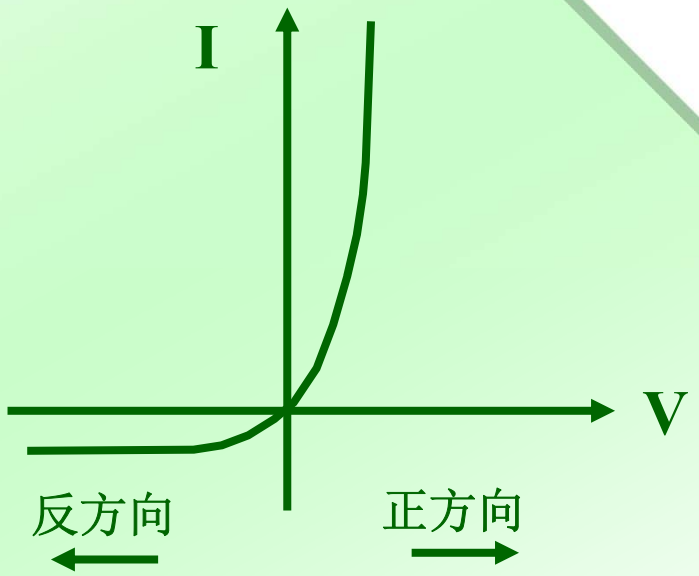
1. 二极管 （PN结）

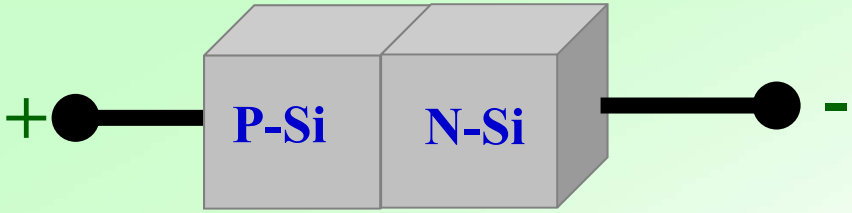
电路符号：

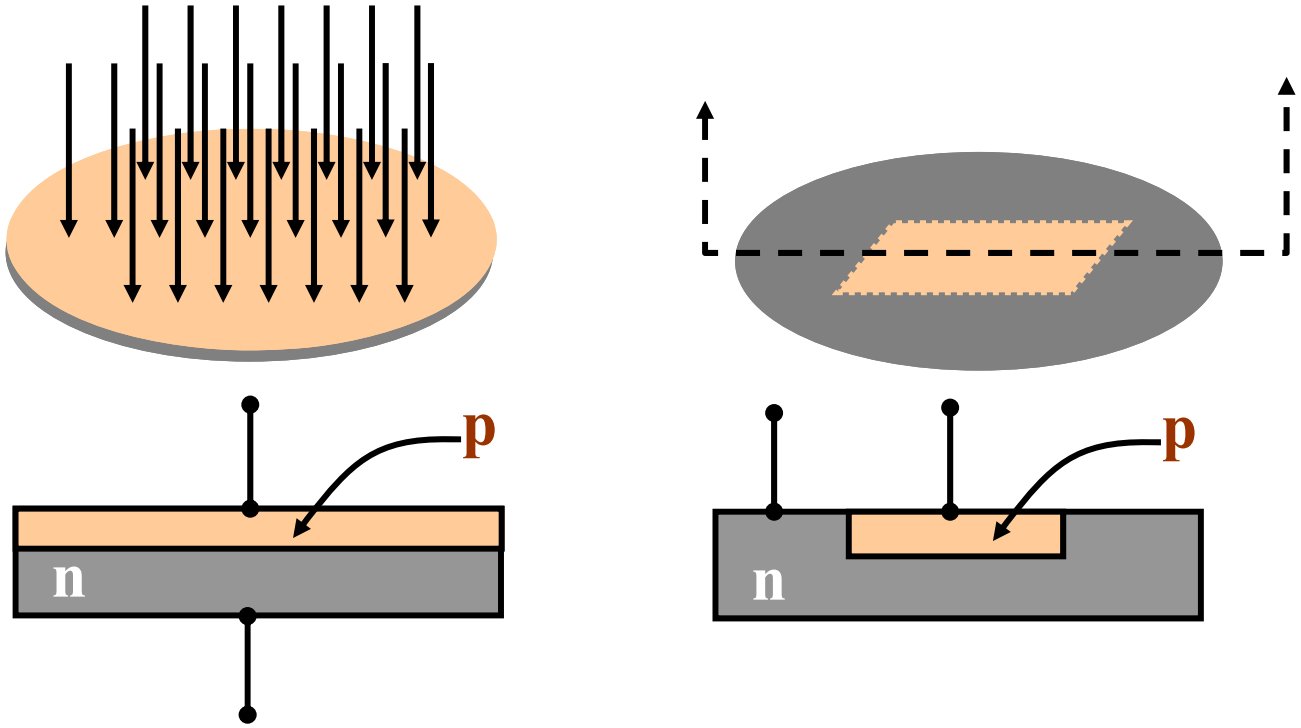

有电流流过


没有电流流过

对于硅二极管，正方向的
电位差与流过的电流大小
无关，始终保持0.6V-0.7V





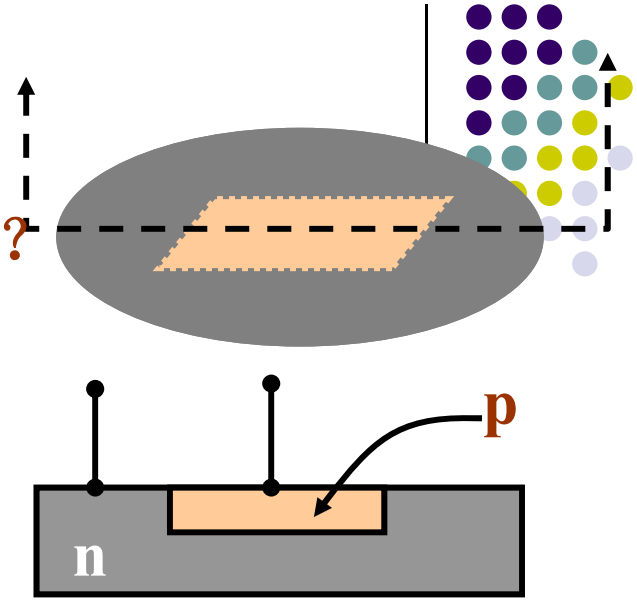


$$I = q\left(\frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0}\right)\left(e^{qVF/KT} - 1\right)A$$

问题：

1.完成一个二极管  需要几块掩模板？

2.这些掩模板应该如何设计？

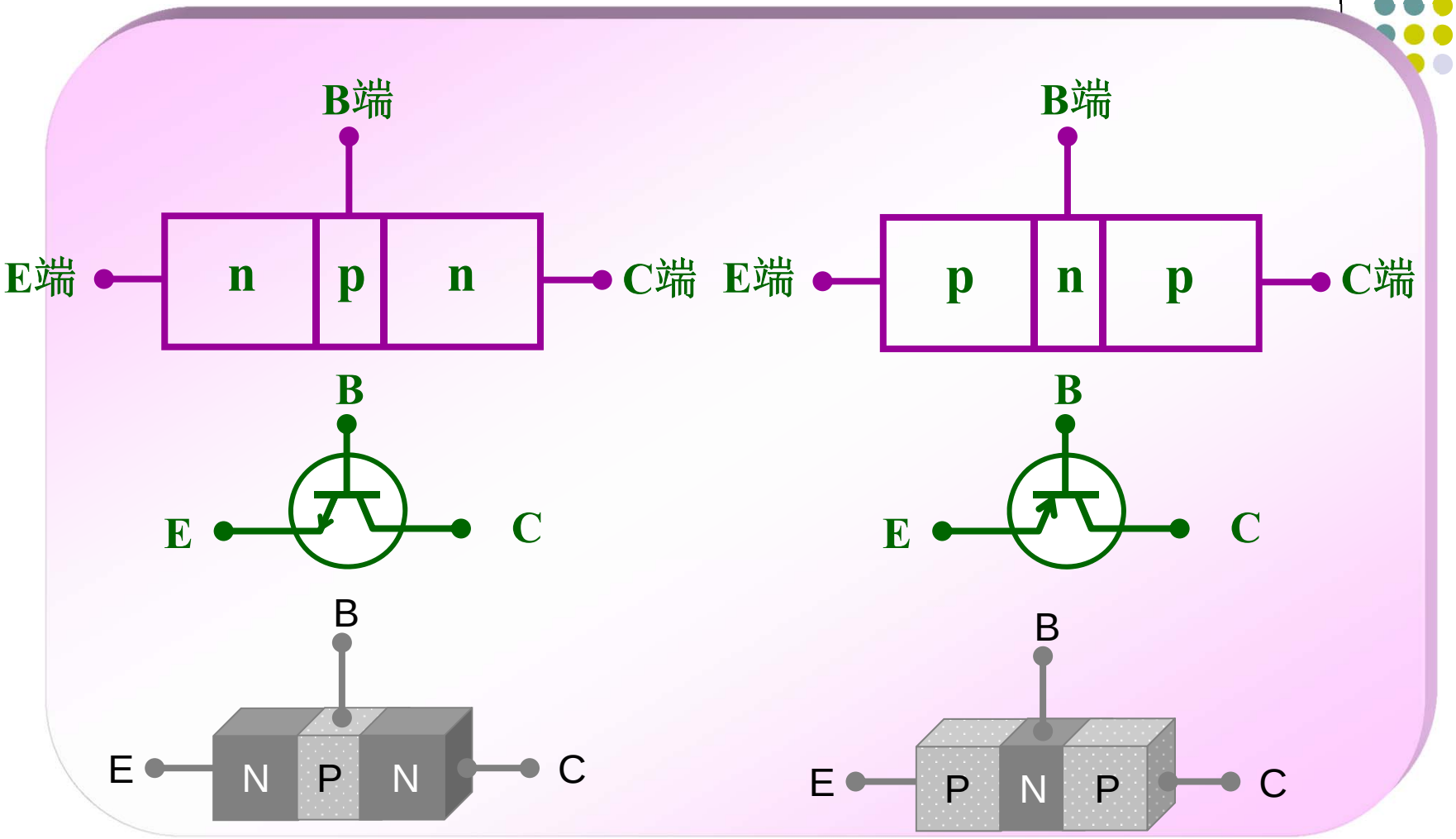


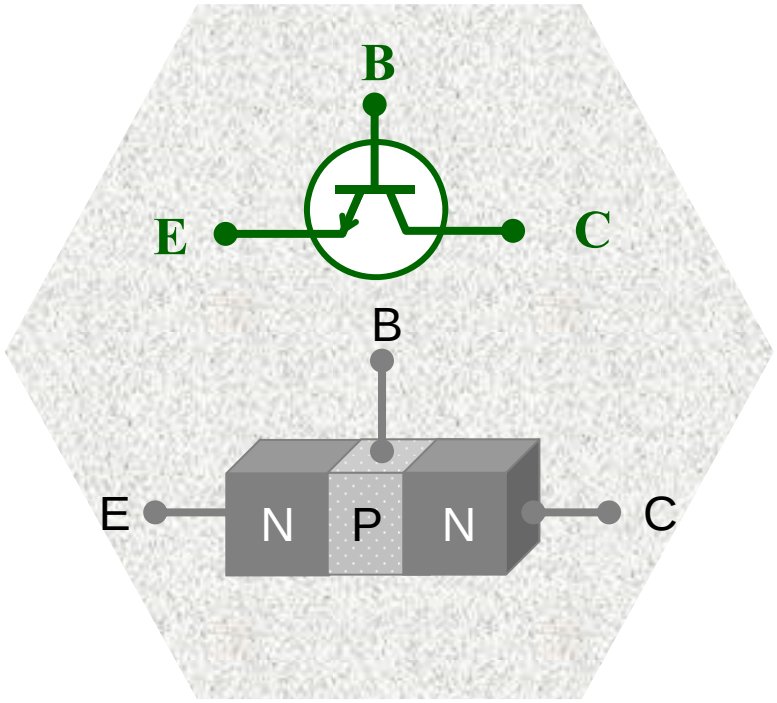
$$I = q(\frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0})(e^{qVF/KT} - 1)A$$

设计者的任务：

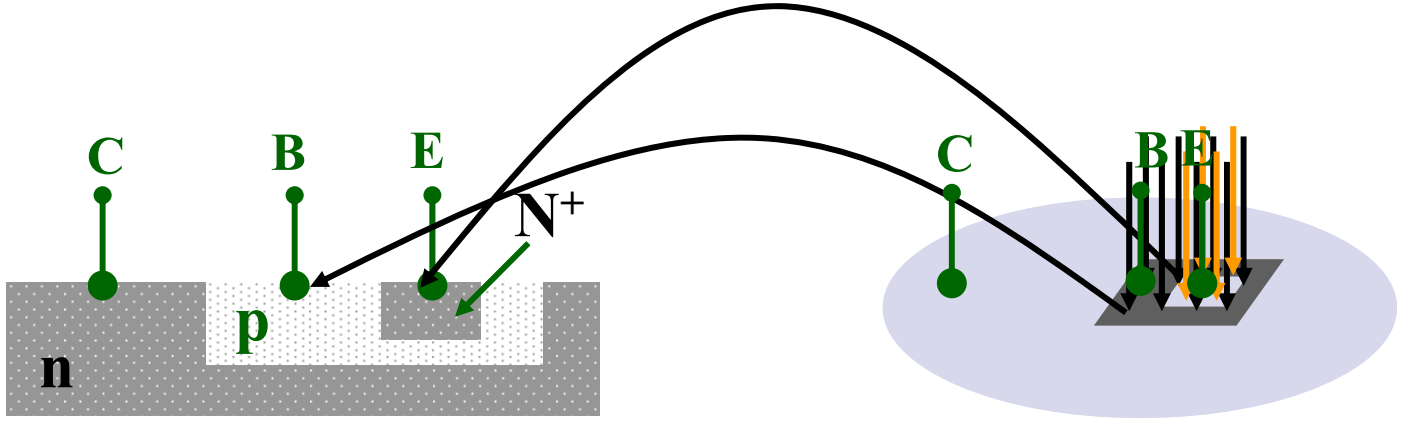
根据工艺可以提供的相关参数，计算达到设计指标时的二极管截面积

2. 双极型 晶体管

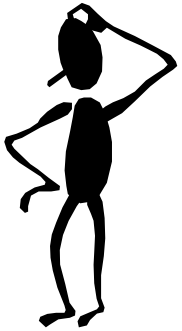


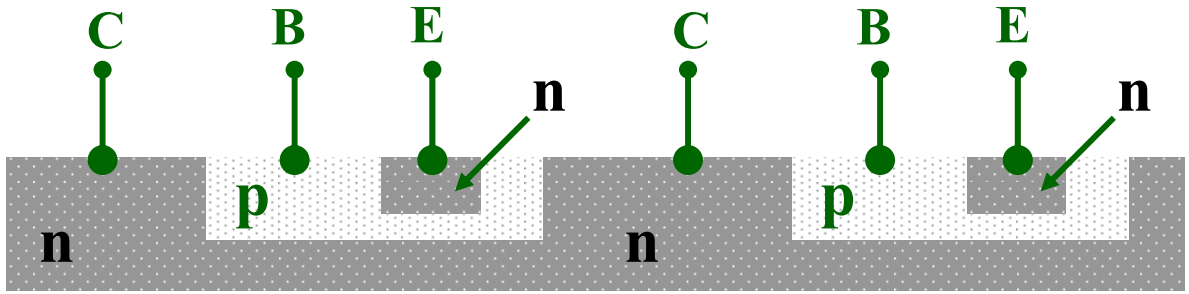

B
E
C
B
E
N
P
N
C

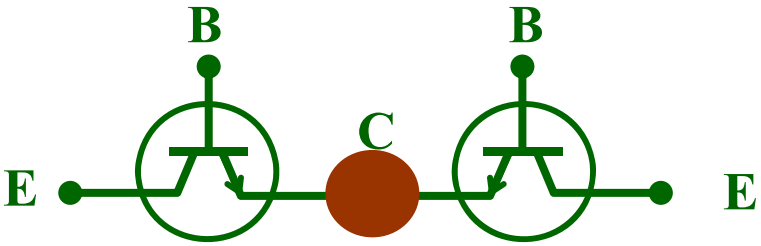

?

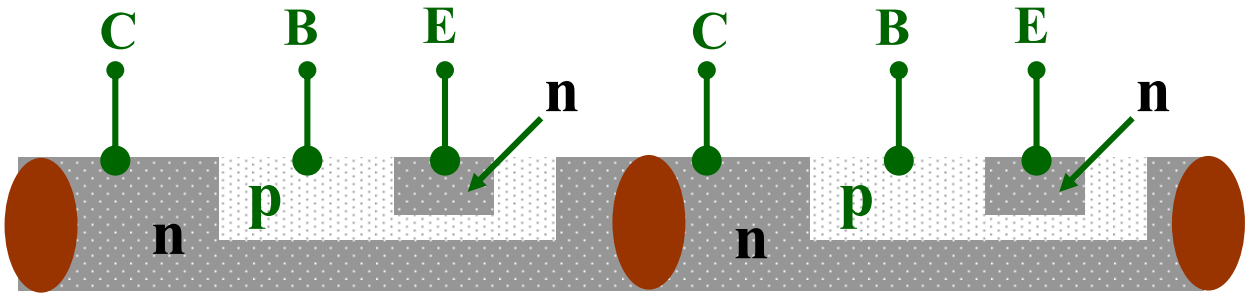

C
B
E
N+
C
B
E
p
n

双极集成电路中元件的隔离



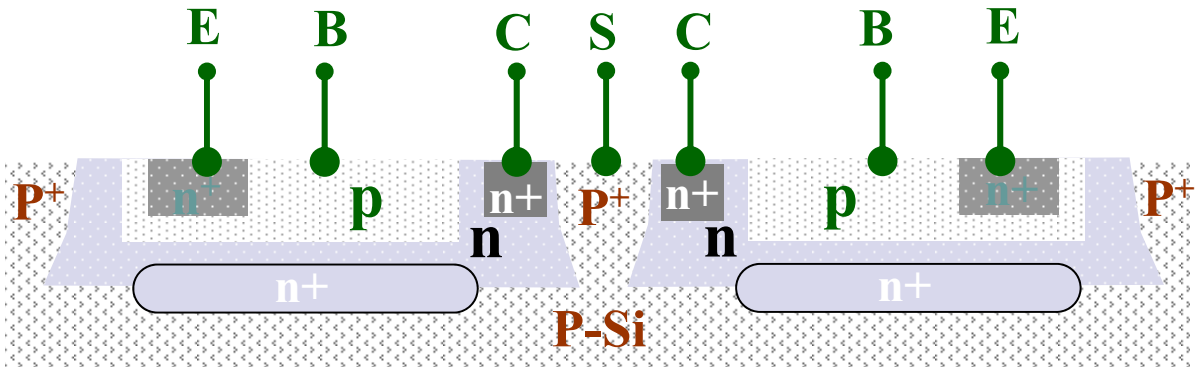






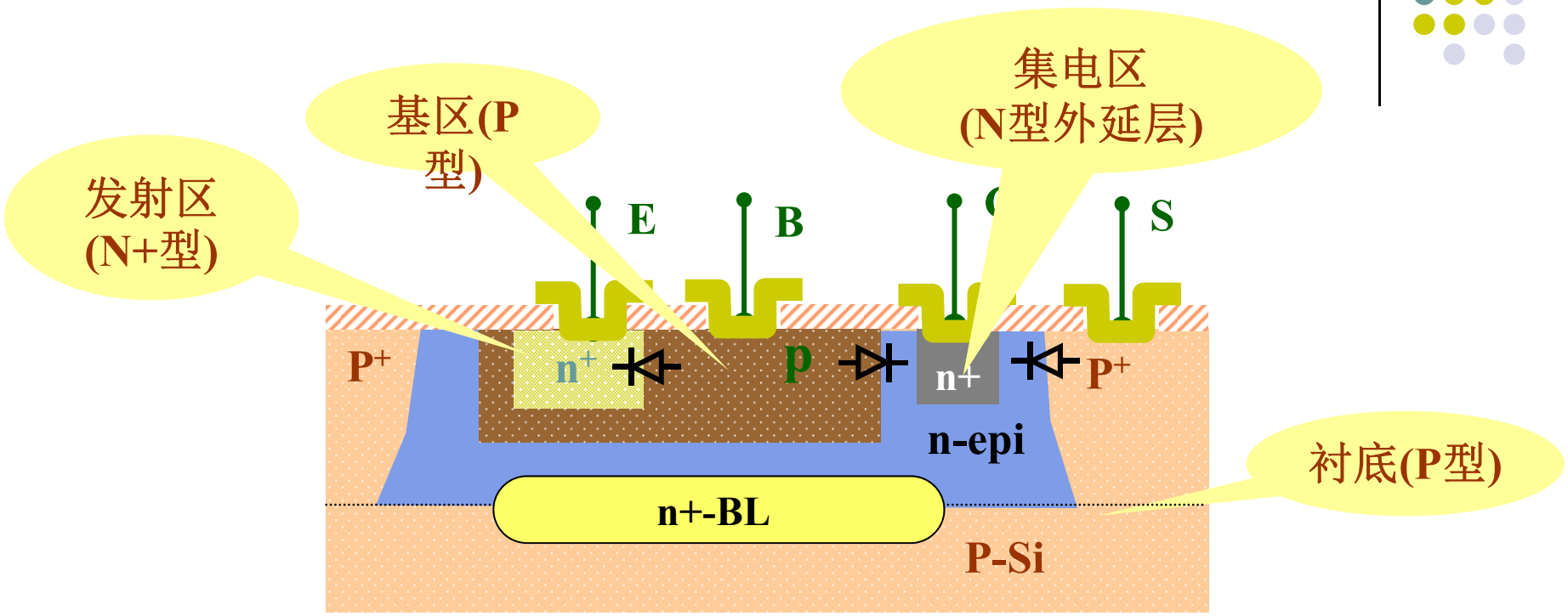
介质隔离

PN隔离



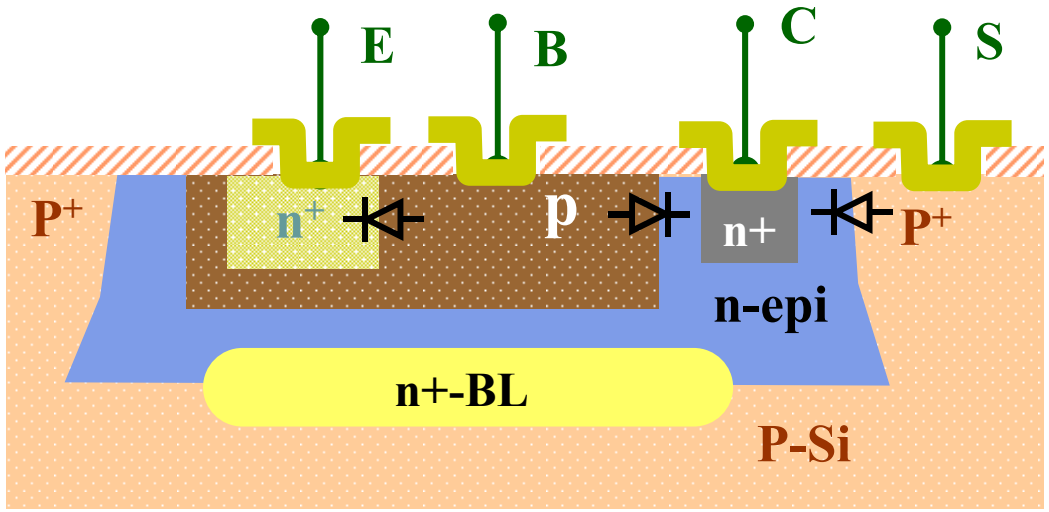
双极集成电路中元件的隔离

双极集成电路元件的形成过程、结构和寄生效应



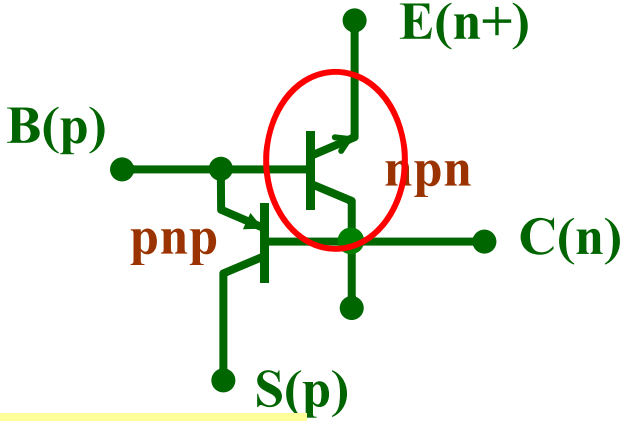
四层三结结构的双极晶体管

双极集成电路元件断面图



衬底接最低电位

等效电路

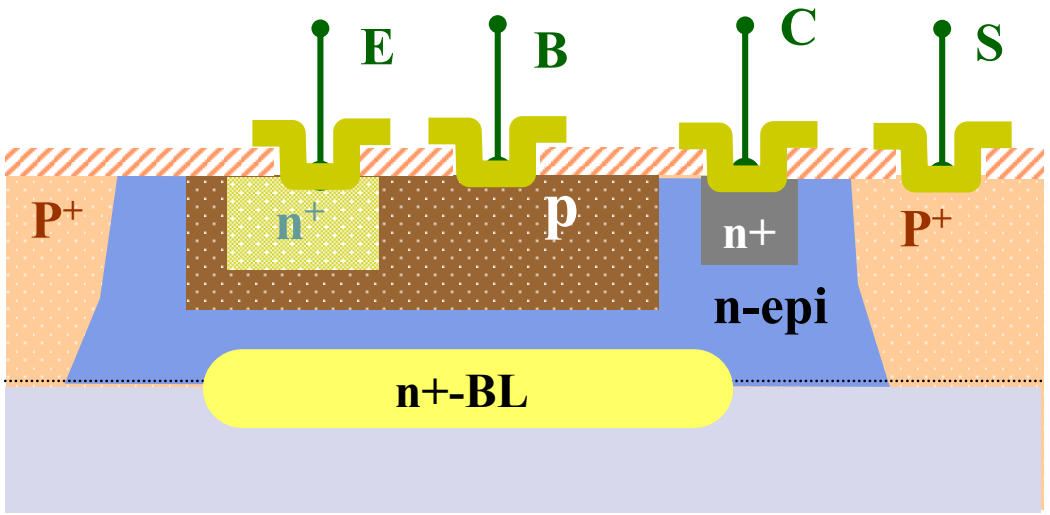


隐埋层作用：
1. 减小寄生pnp管的影响
2. 减小集电极串联电阻

双极集成电路等效电路

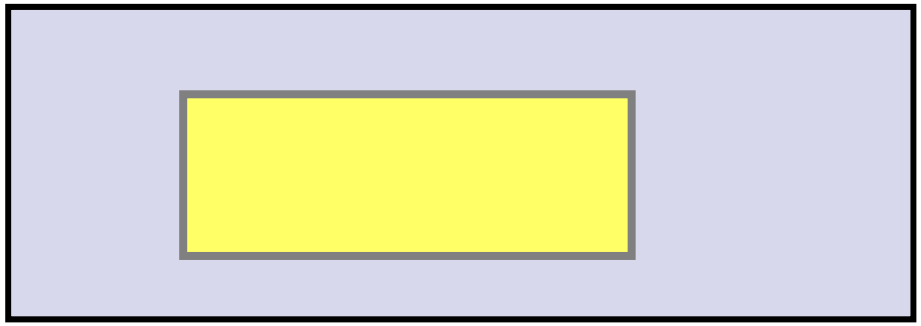
1:衬底选择

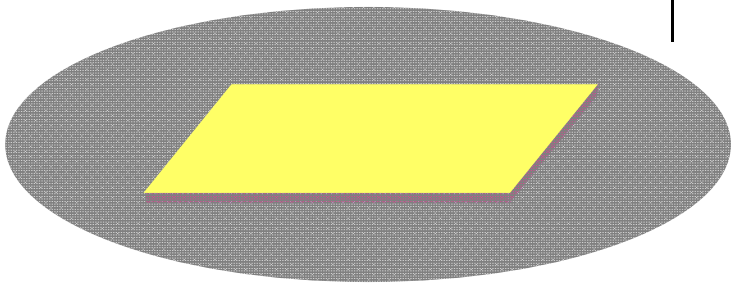
- 确定衬底材料类型 ➡ P型硅(p-Si)
- 确定衬底材料电阻率 ➡ ρ≈10Ω.cm
- 确定衬底材料晶向 ➡ （111）偏离2~5^0

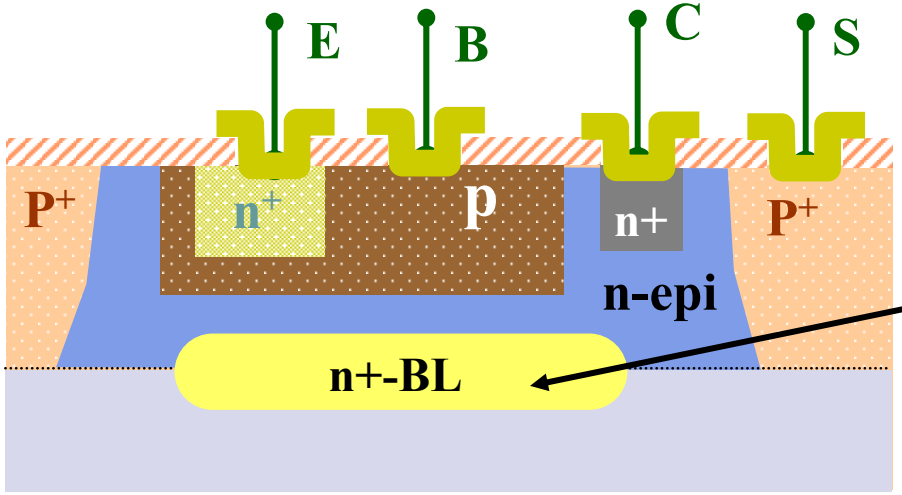


典型PN结隔离双极集成电路中元件的形成过程

2:第一次光刻----N+隐埋层扩散孔光刻







典型PN结隔离双极集成电路中元件的形成过程

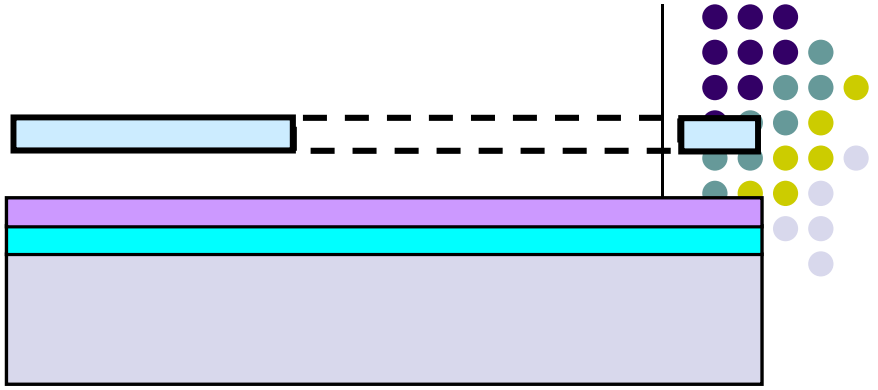
具体步骤如下：

1．生长二氧化硅（湿法氧化）：

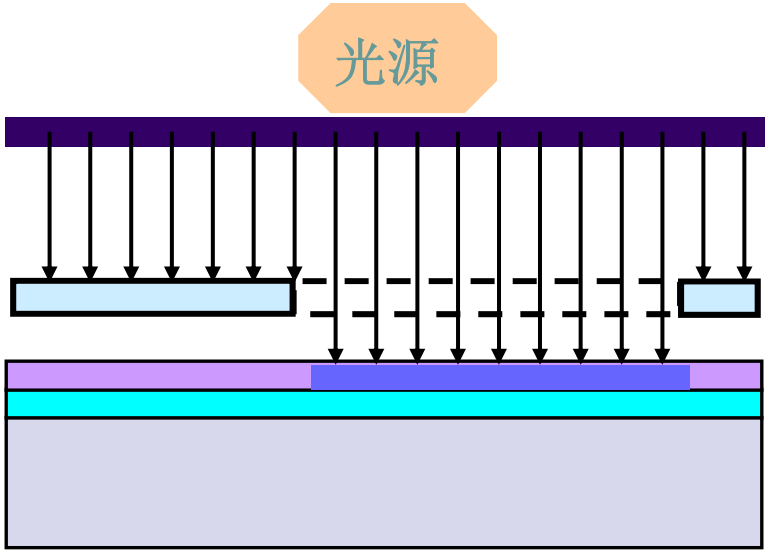
$$Si(固体)+ 2H_2O \rightarrow SiO_2（固体）+2H_2$$

2. 隐埋层光刻：

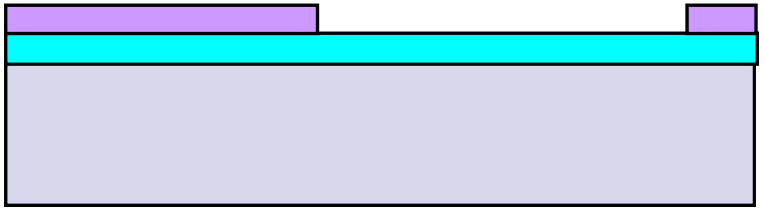
涂胶



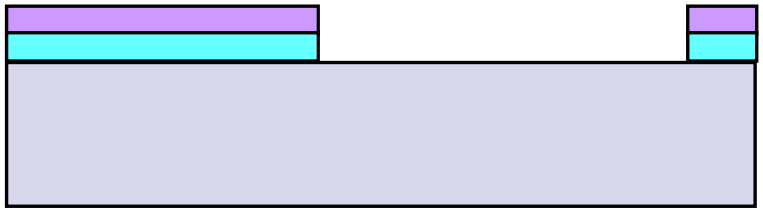
掩膜对准



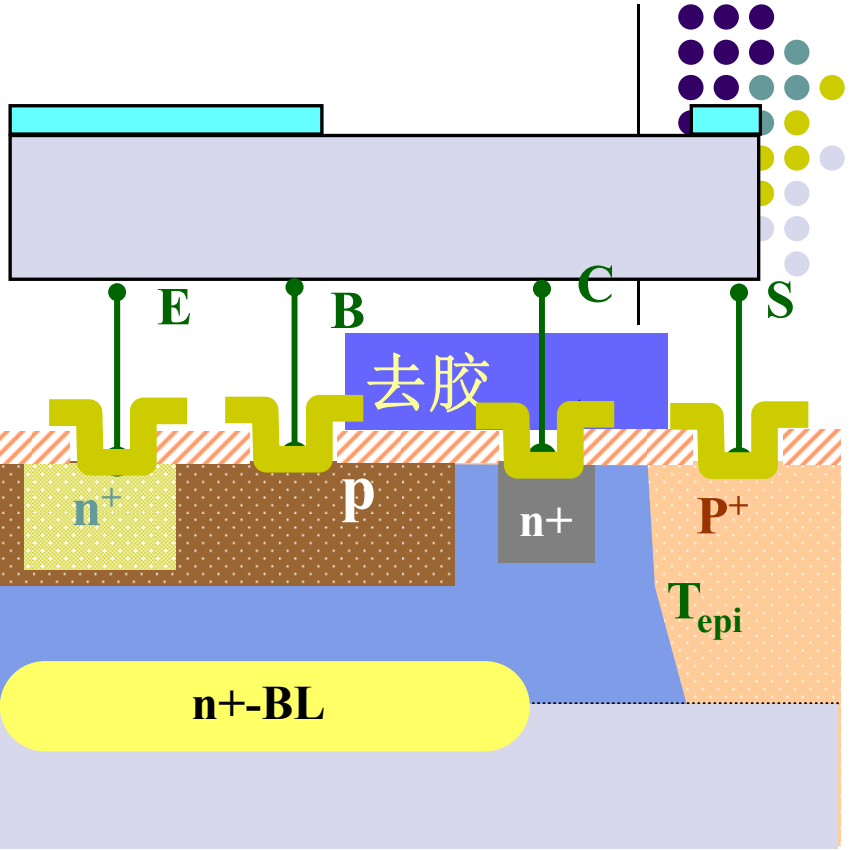
曝光



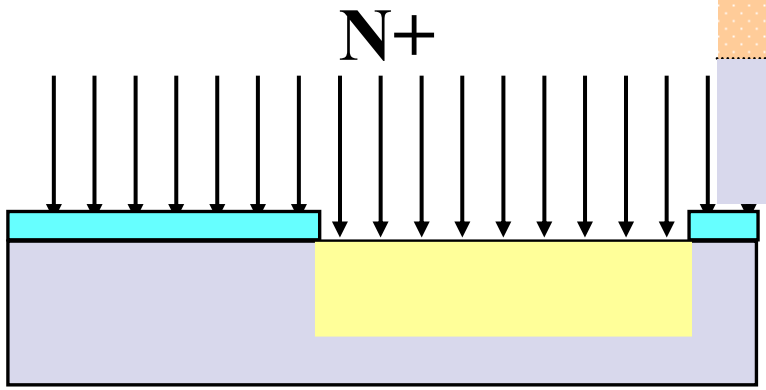
显影



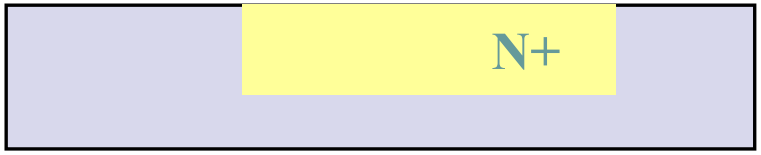
刻蚀（等离子体刻蚀）



3．N+掺杂：



As掺杂（离子注入）

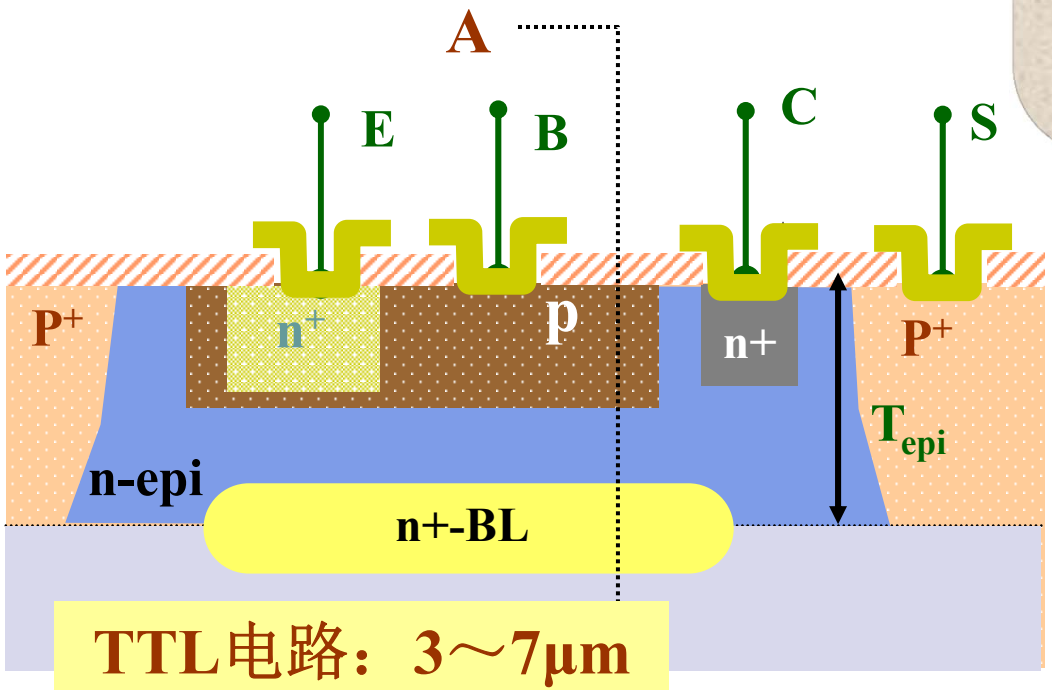


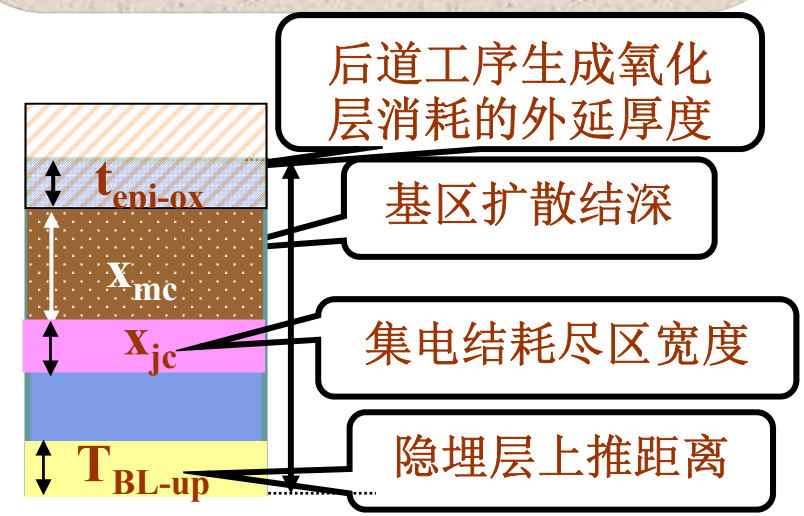
去除氧化膜

3:外延层

主要设计参数

- 外延层的电阻率ρ;
- 外延层的厚度T_{epi};



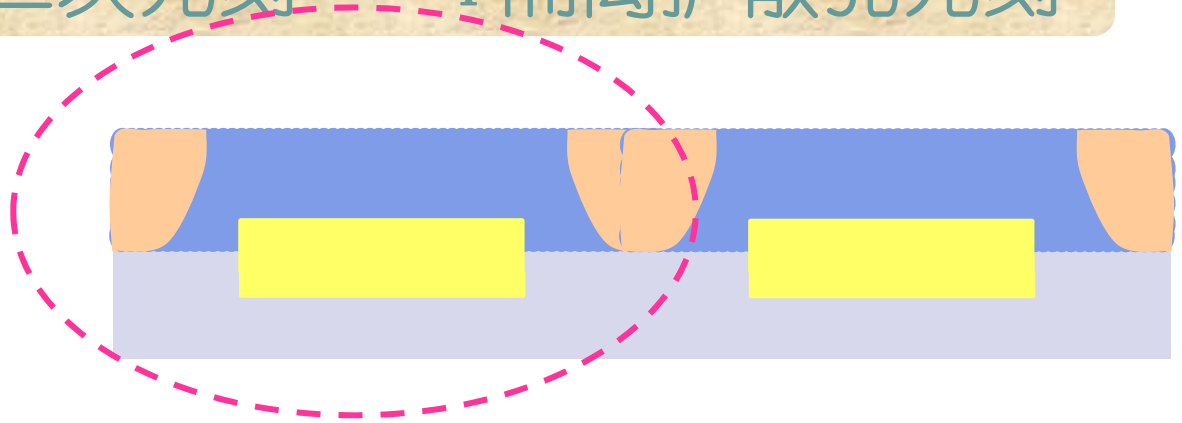


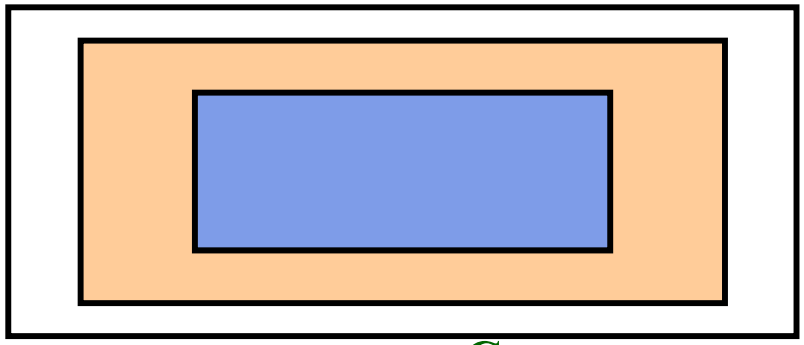
TTL电路：3～7μm
模拟电路：7～17μm

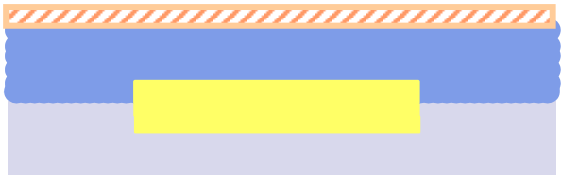
$T_{epi} > x_{jc}+x_{mc}+T_{BL-up}+t_{epi-ox}$

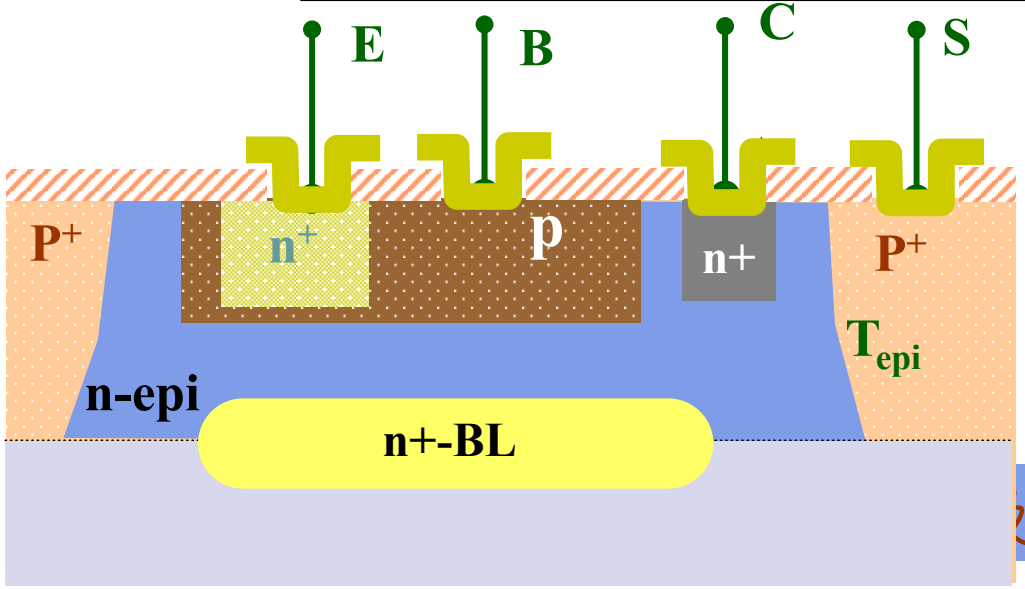
典型PN结隔离双极集成电路中元件的形成过程

4:第二次光刻----P隔离扩散孔光刻



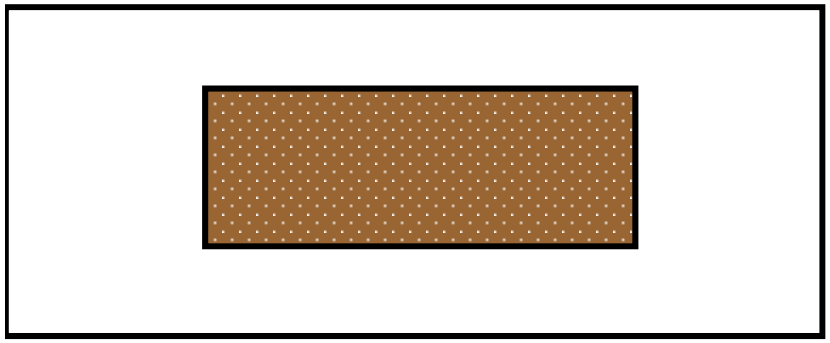


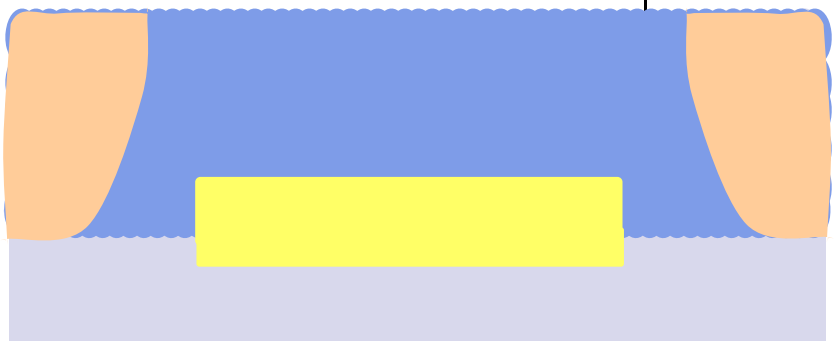


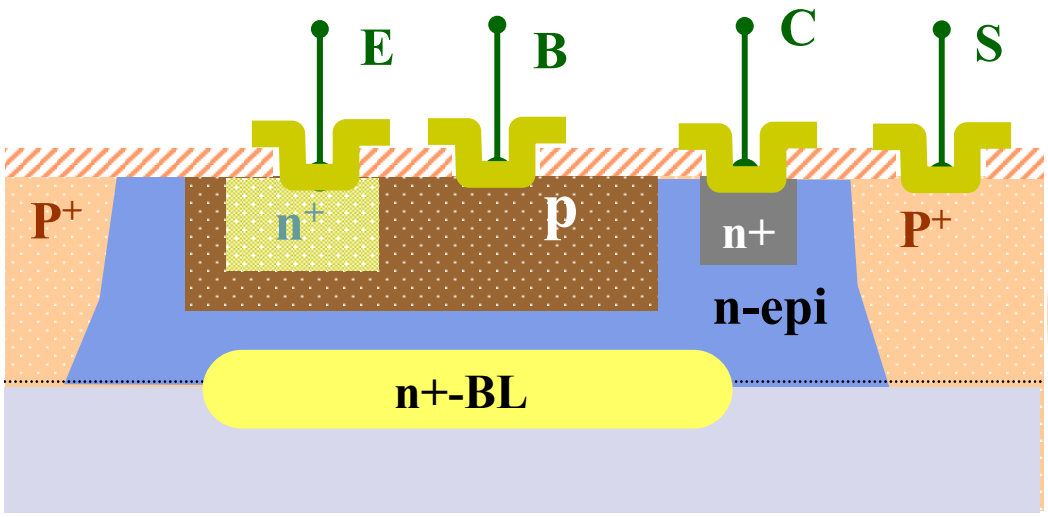


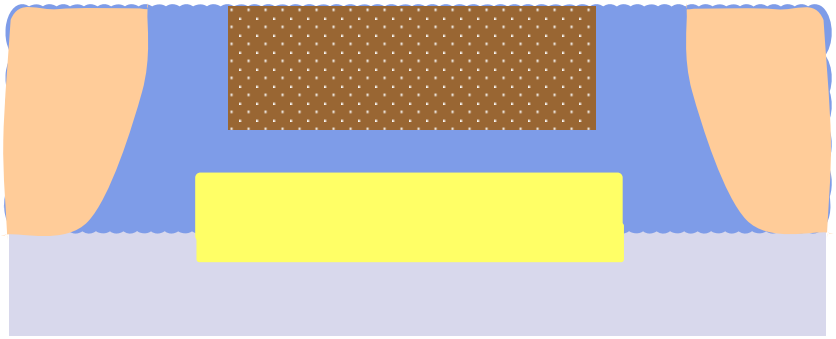
集成电路中元件的形成过程

5:第三次光刻----P型基区扩散孔光刻



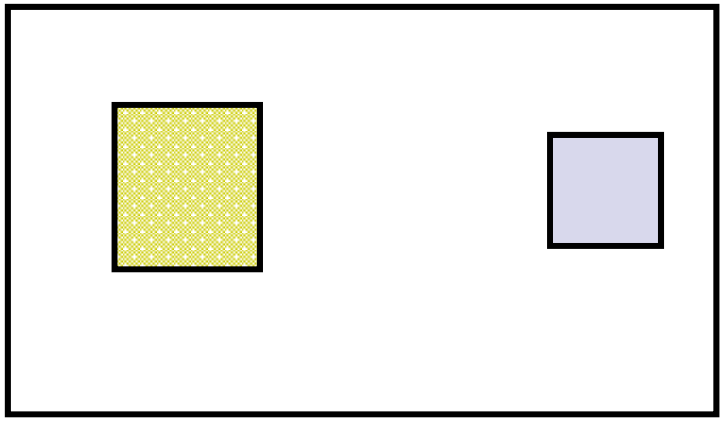


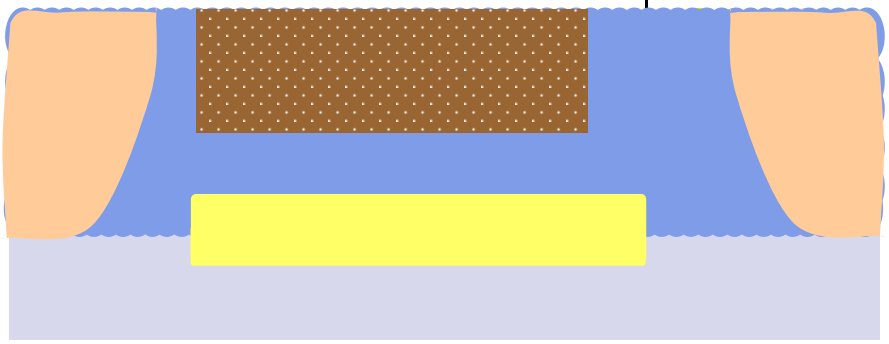


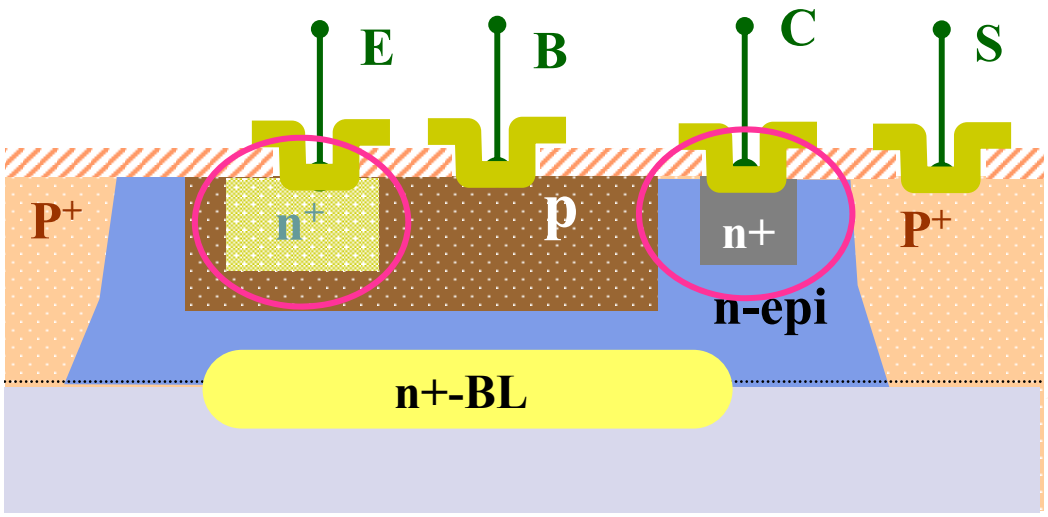


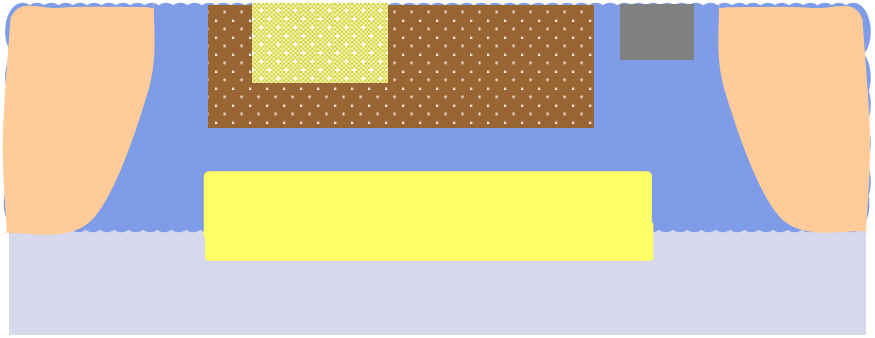
典型PN结隔离双极集成电路中元件的形成过程

6:第四次光刻----N+发射区扩散孔光刻



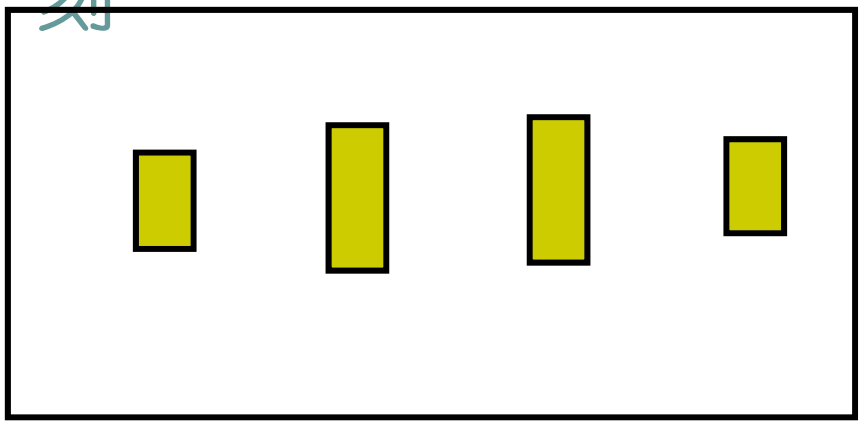


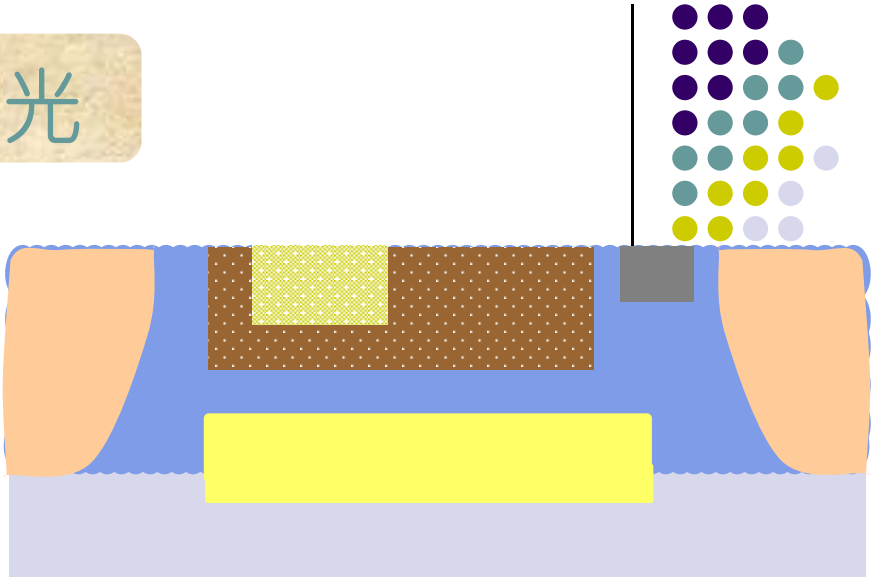


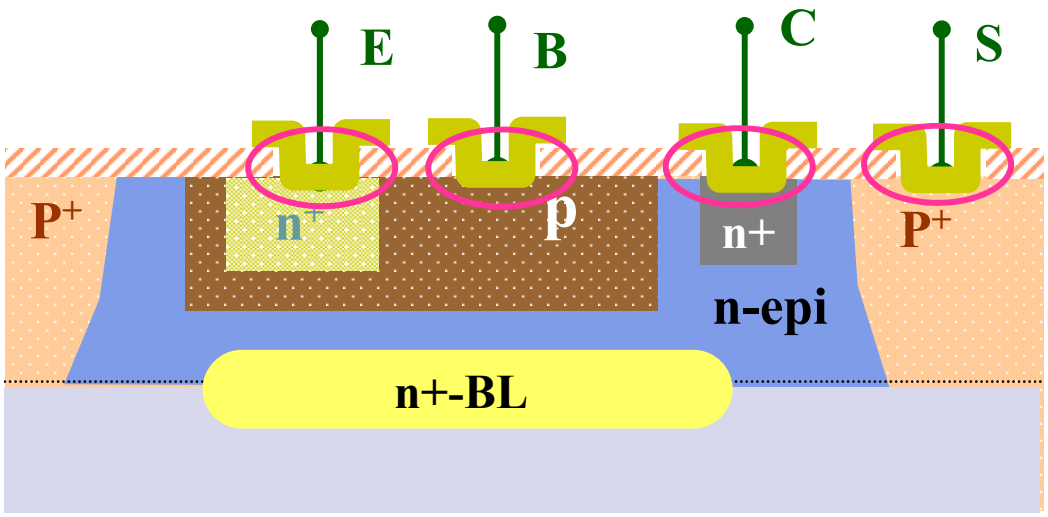


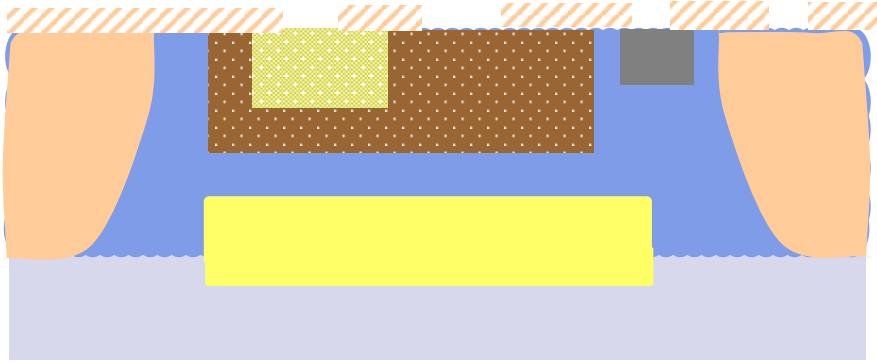
典型PN结隔离双极集成电路中元件的形成过程

7:第五次光刻-----引线孔光刻



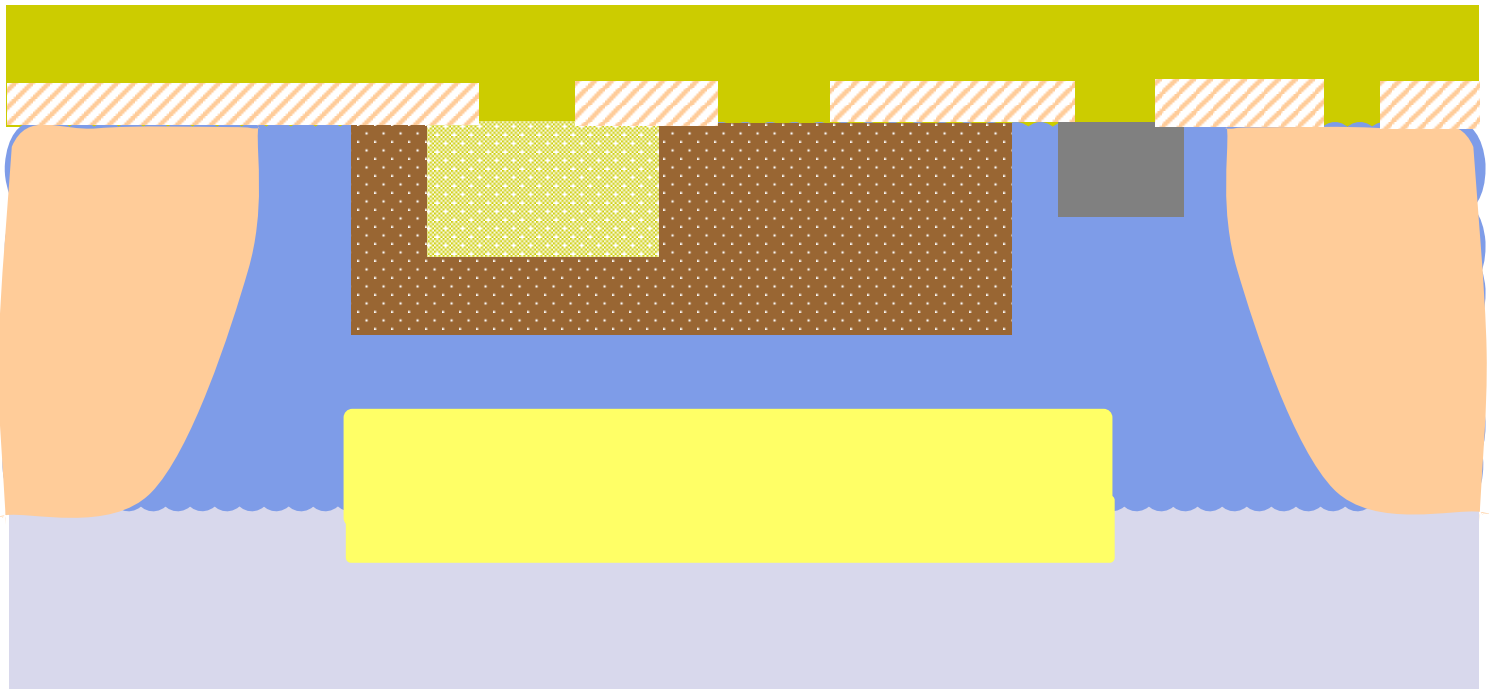






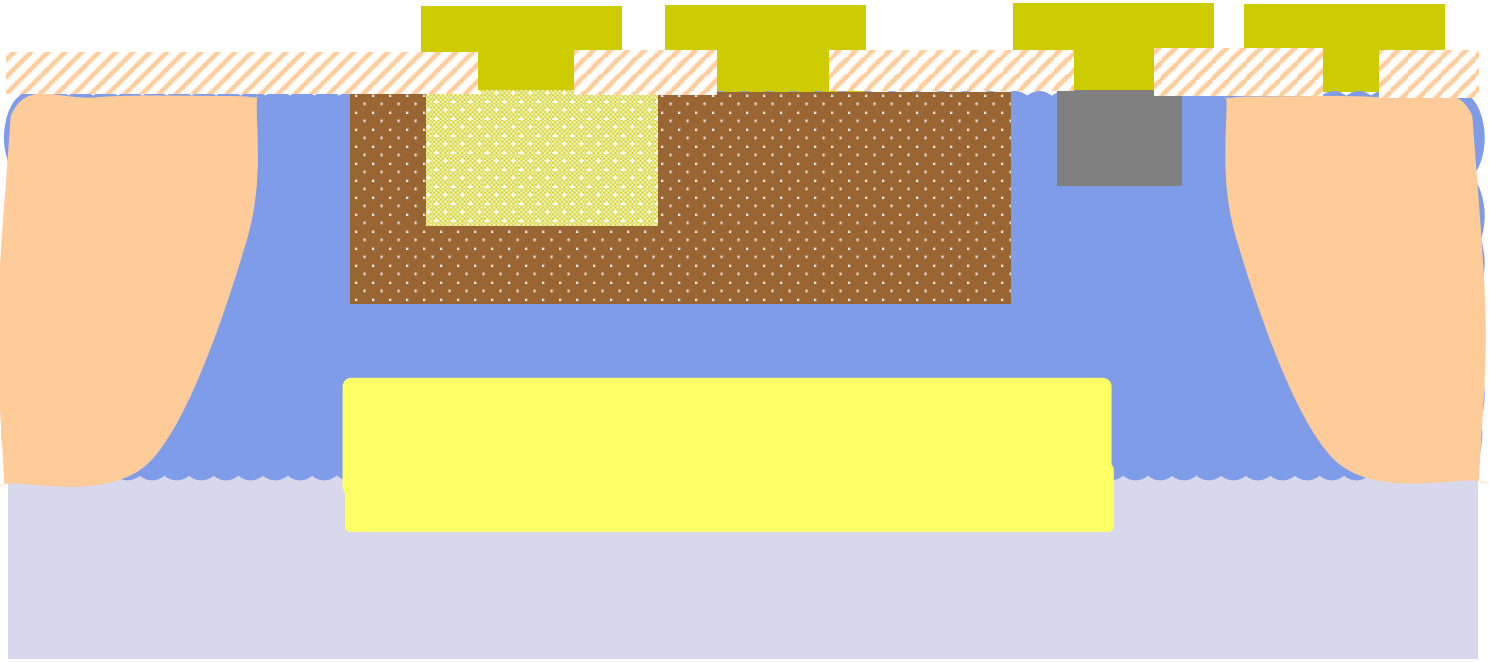
典型PN结隔离双极集成电路中元件的形成过程

8:铝淀积

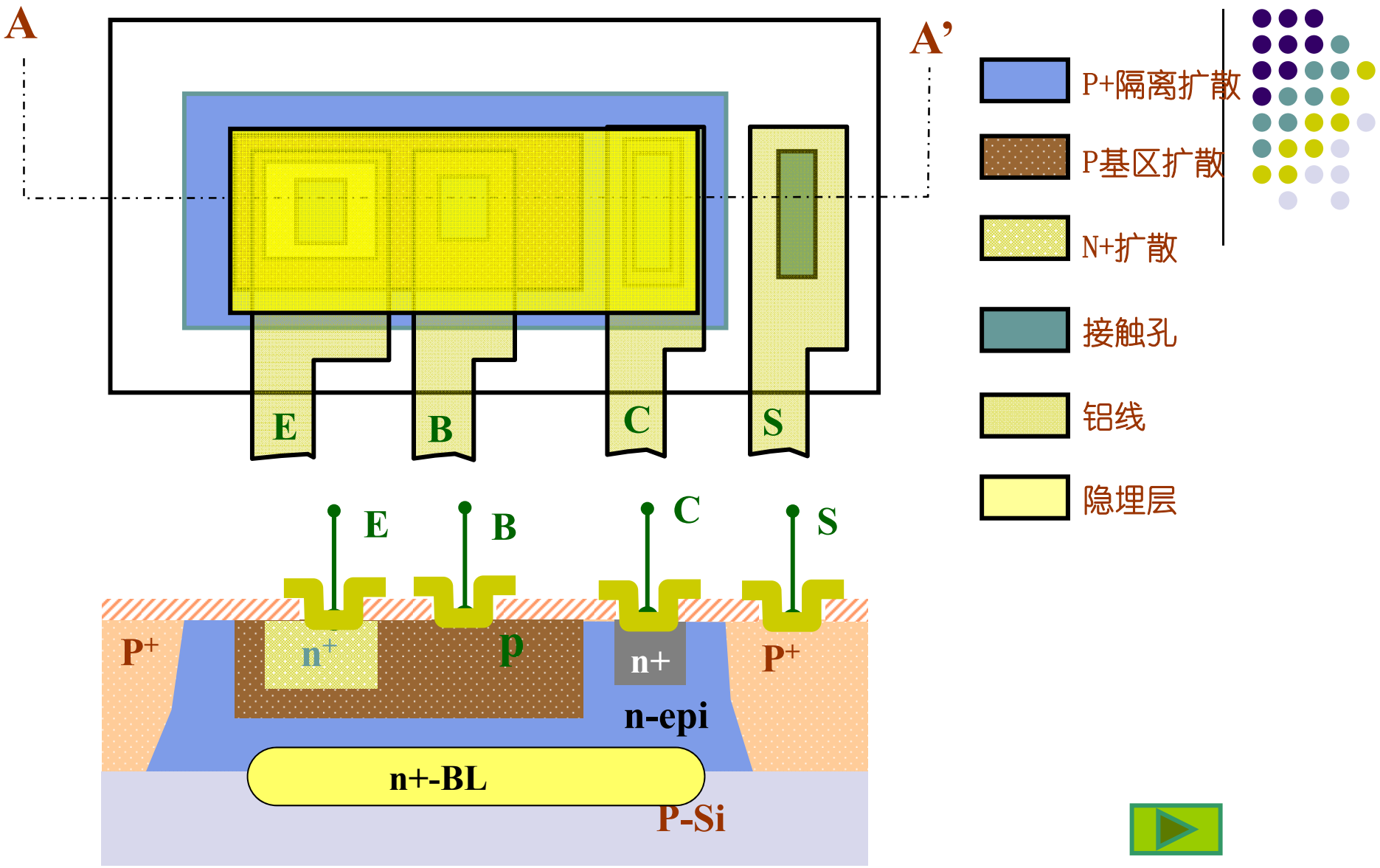


典型PN结隔离双极集成电路中元件的形成过程

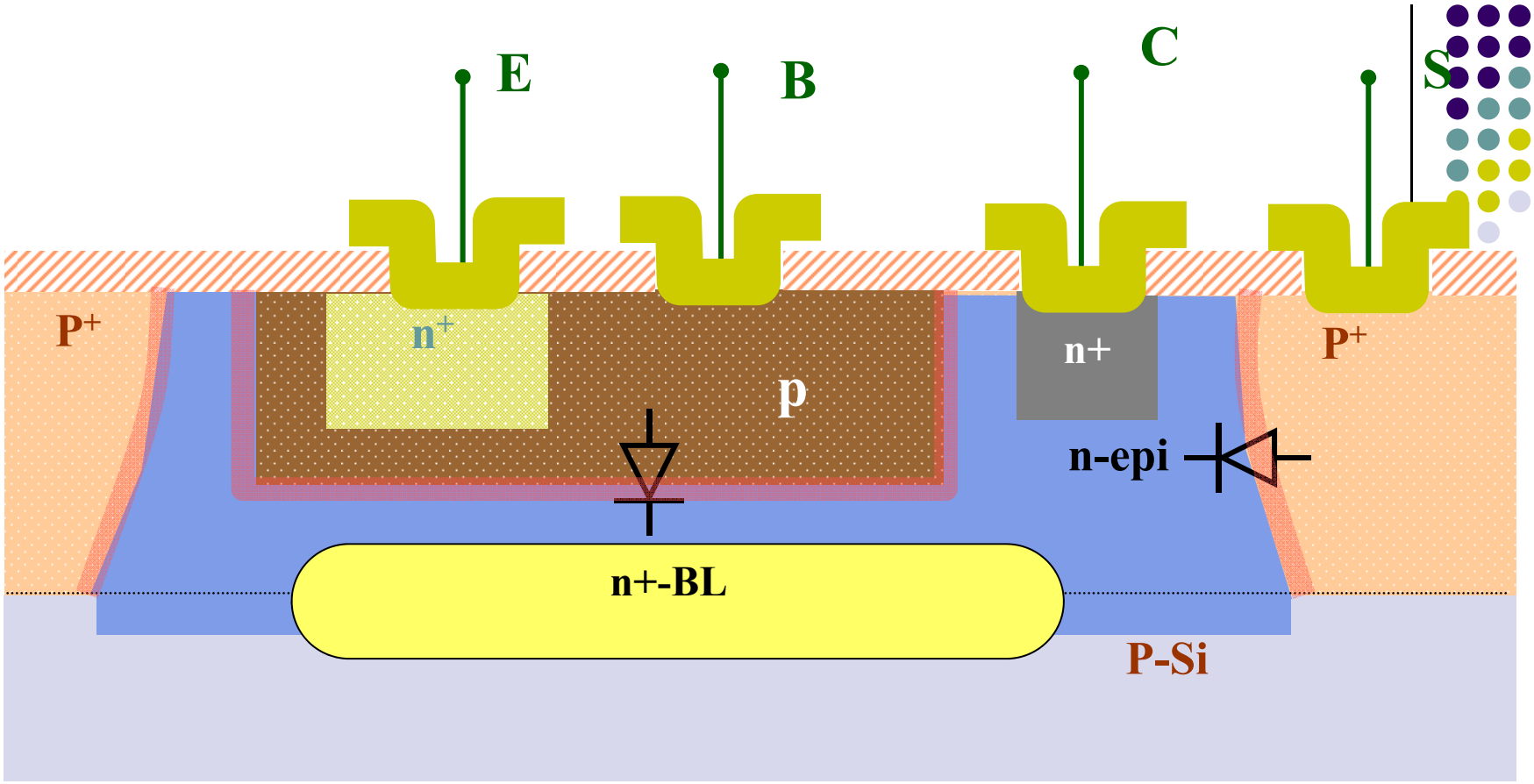
9:第六次光刻----反刻铝



典型PN结隔离双极集成电路中元件的形成过程



双极集成电路元件断面图



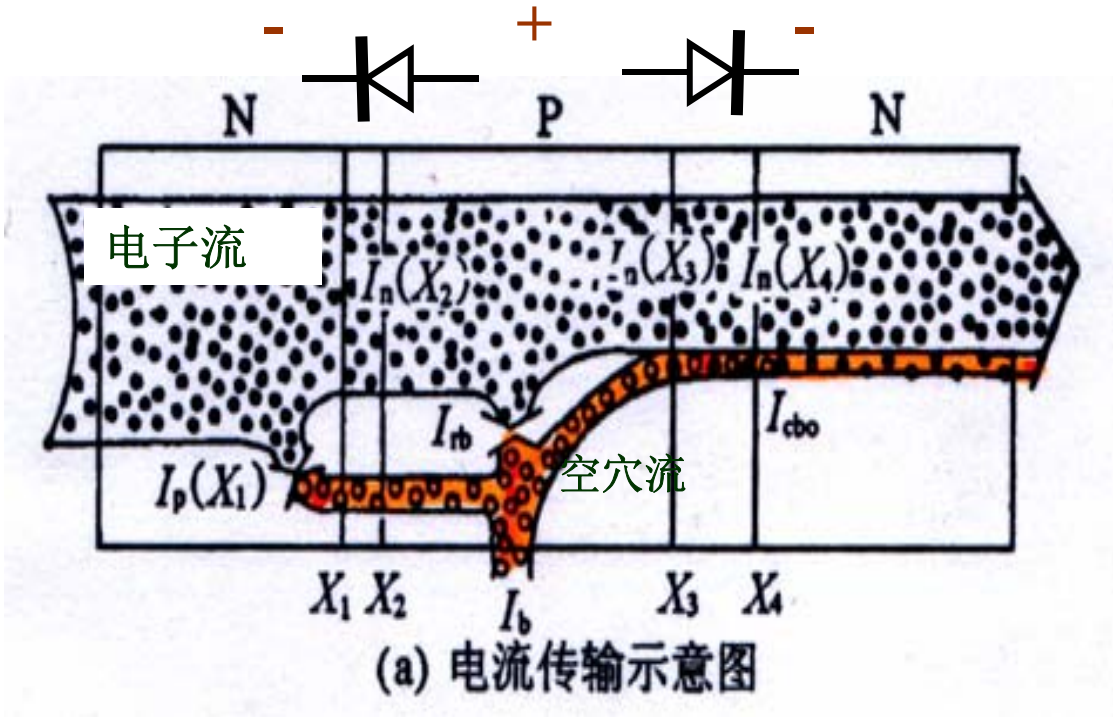
为了减小结电容,击穿电压高，外延层下推小,电阻率应取大;

为了减小集电极串联电阻,饱和压降小，电阻率应取小.

TTL电路：0.2Ω.cm
模拟电路：0.5～5Ω.cm

折中

思考：



(a) 电流传输示意图

$$I_c = \alpha I_e + I_{cbo} \approx \alpha I_e$$

$$I_c \approx \beta I_b$$

α由什么决定？

$$I = q\left(\frac{D_n}{L_n} n_{p0} + \frac{D_p}{L_p} p_{n0}\right)\left(e^{qVF/KT} - 1\right)A$$

作业:

1. 画出NPN晶体管的版图，并标注各区域的掺杂类型（直接在图上标），写出实现该NPN晶体管至少需要多少次光刻以及每次光刻的目的。每一块光刻板图形的尺寸应该如何设计？

2. 画出下图示例在A-A',B-B' C-C'处的断面图。