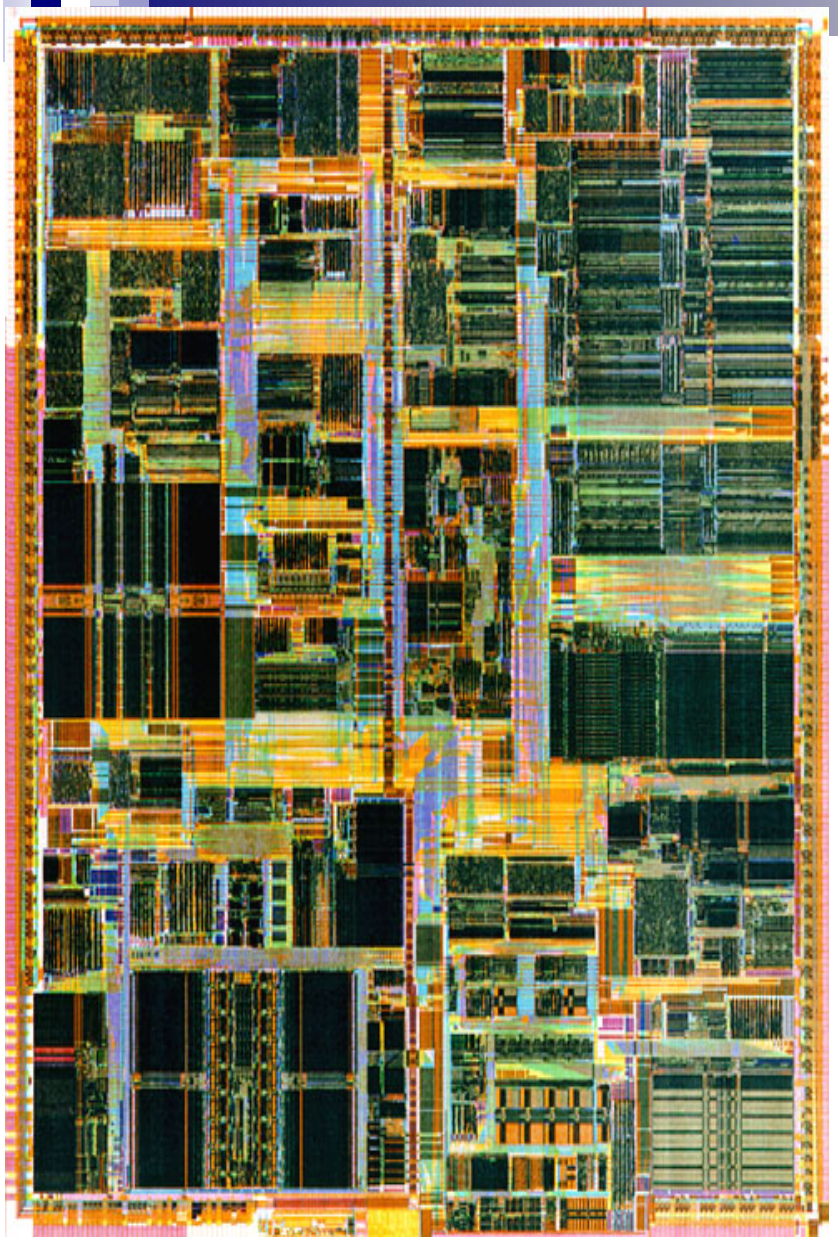


半导体集成电路

学校：西安理工大学
院系：自动化学院电子工程系
专业：电子、微电
时间：秋季学期

2012/11/27

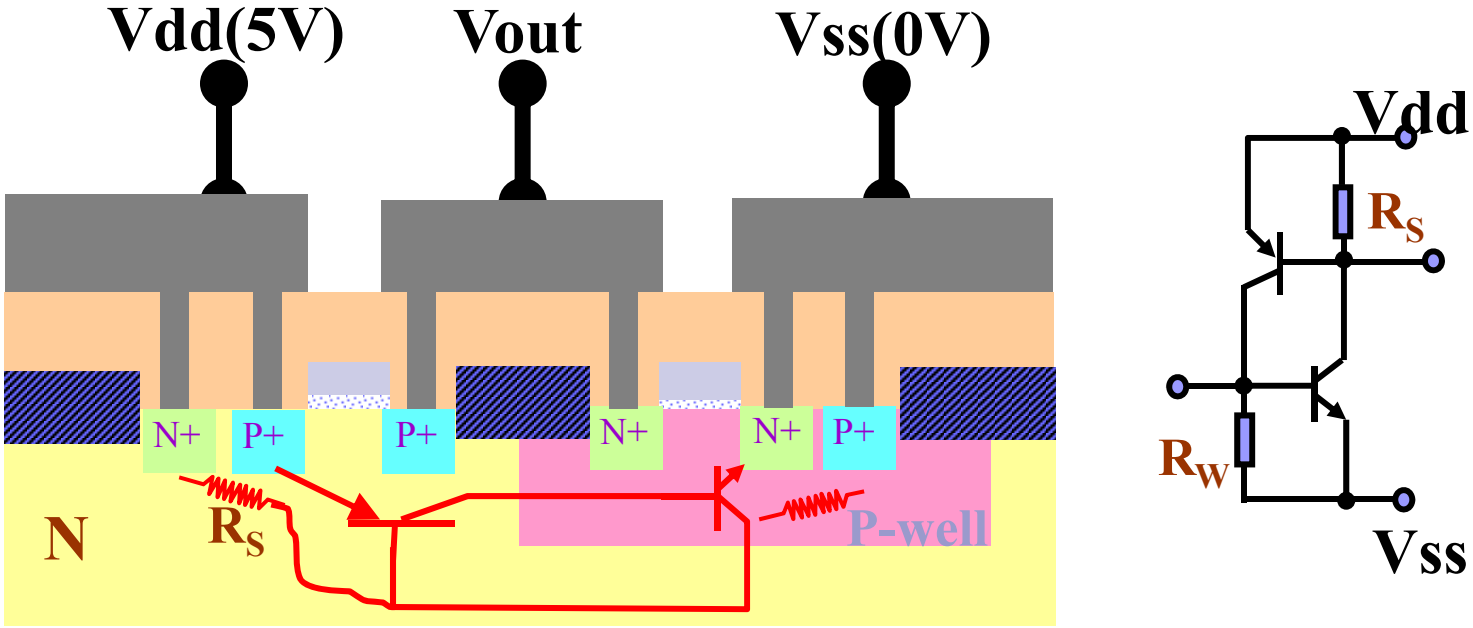
上节课内容要点

- CMOS集成电路的有源寄生效应
- 集成电路中的无源元件
  - ➢集成电阻器
  - ➢集成电容器

◆基本要求

◆基本要求

- CMOS有源寄生产生的原因及减弱措施

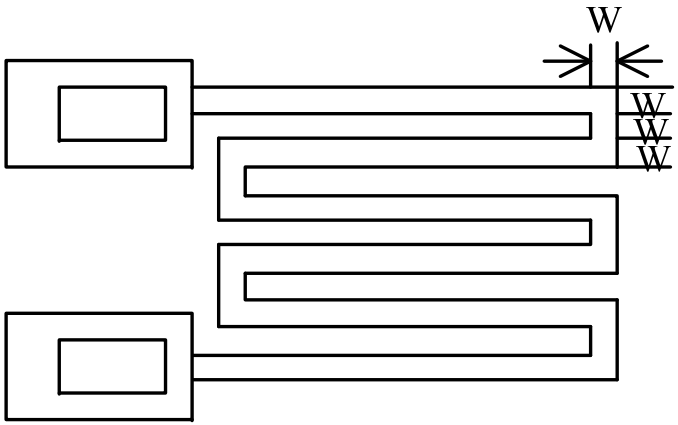


消除措施：

1. 减小R_S,R_W（增加接触孔数量，加粗电源、地线,双阱工艺）

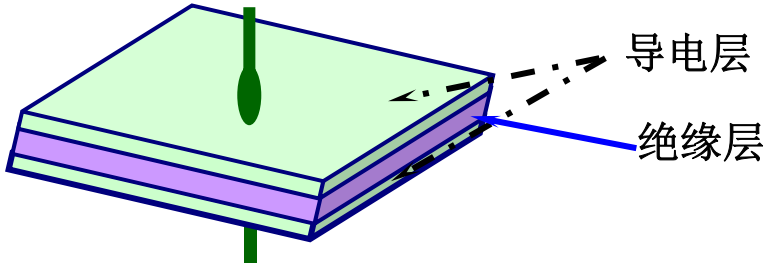
2.降低寄生三极管电流放大倍数

电阻、电容的集成结构及计算方法



1. 端头修正
2. 拐角修正因子
3. 横向扩散修正因子
4. 薄层电阻值Rs的修正

$$R = K_a R_s \left(\frac{L}{W + 0.55x_{jc}} + 2k_1 + nk_2\right)$$

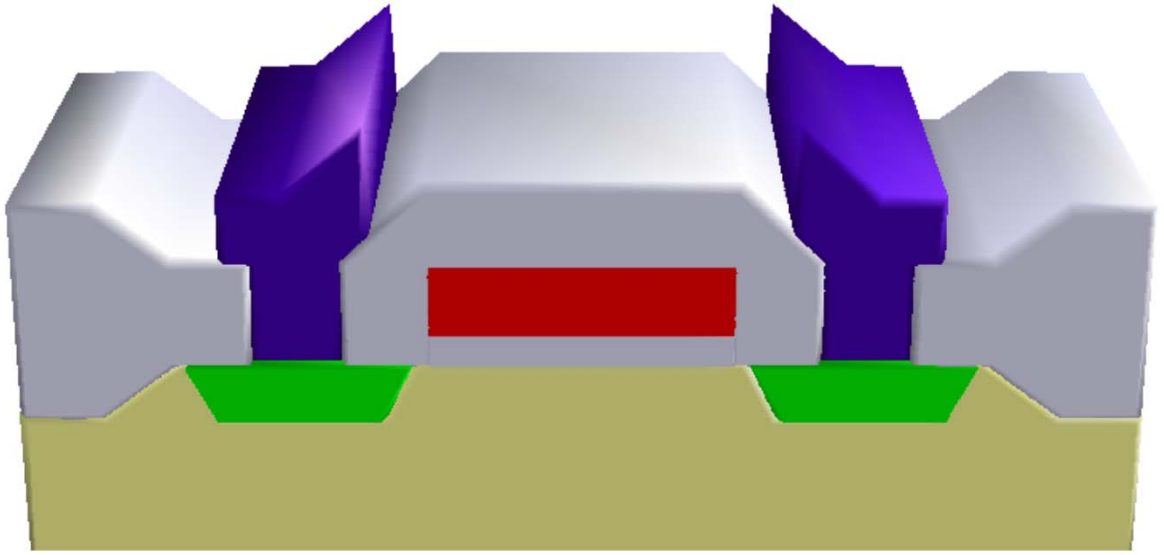


$$C = \frac{\varepsilon}{d} \cdot S \ [F]$$

电阻线宽的设计

1. 设计规则决定最小条宽
2. 工艺水平和精度
3. 流经电阻的最大电流

MOSFET晶体管

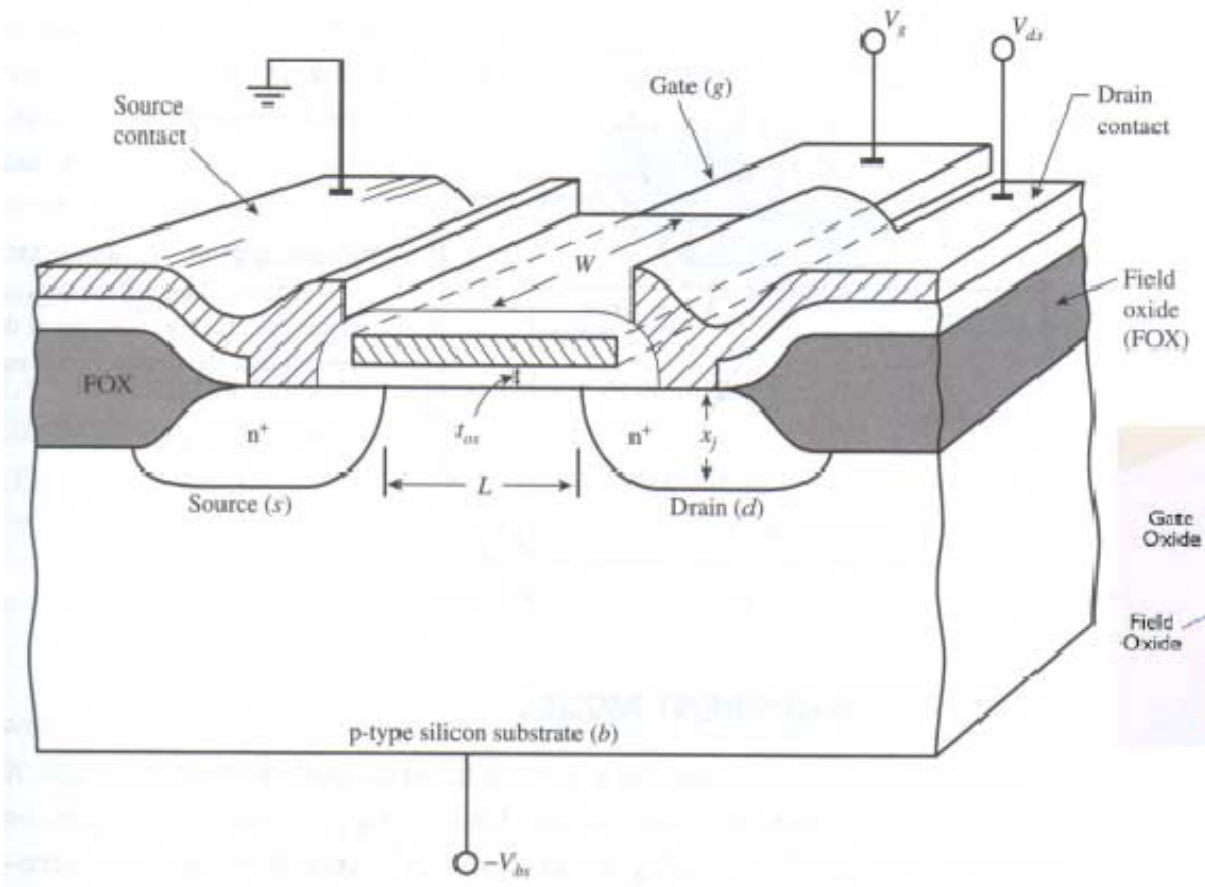


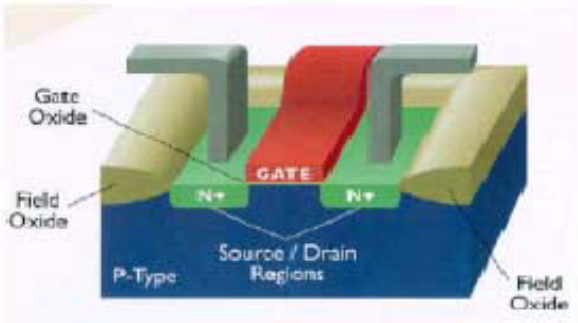
本节课主要内容

- **MOS晶体管**
  - 器件结构
  - 电流方程
  - 电流电压特性
  - 衬底偏压效应
  - 短沟道效应
  - **MOSFET的电容**
  - **MOSFET的导通电阻**

MOSFET

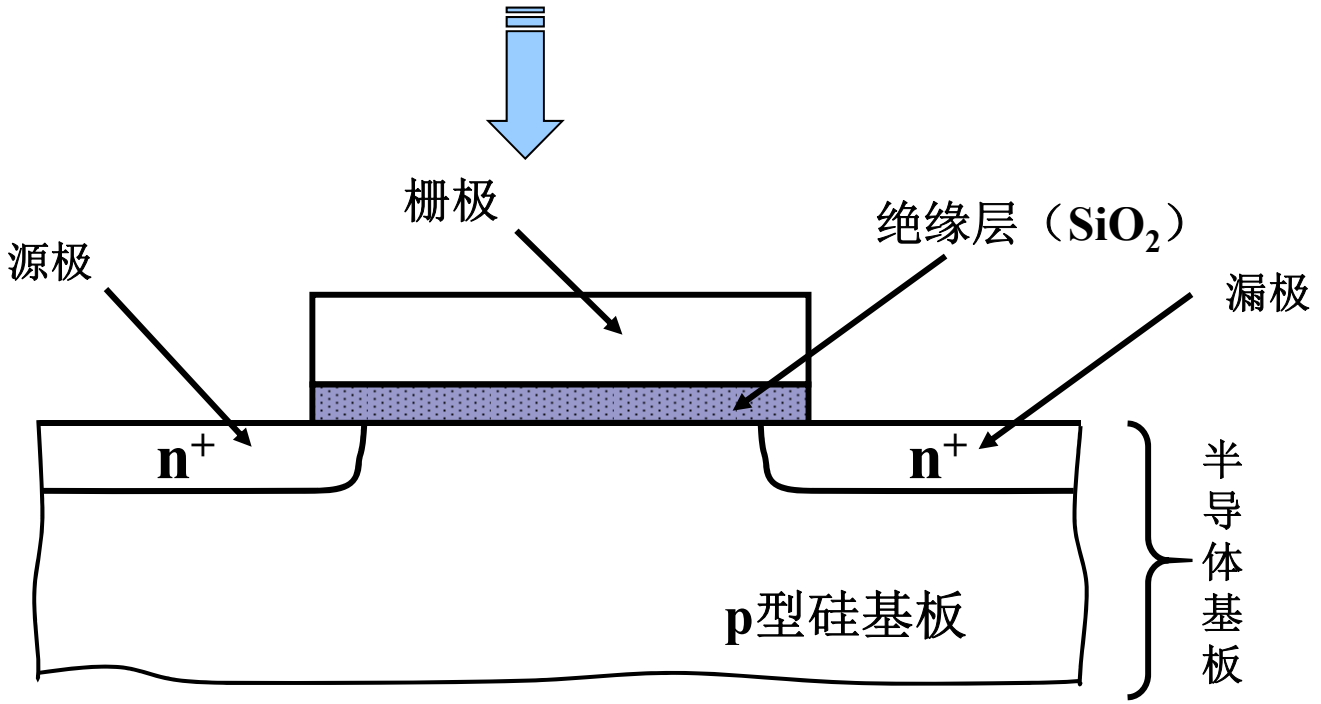
Metal Oxide Semiconductor Field Effect Transistor





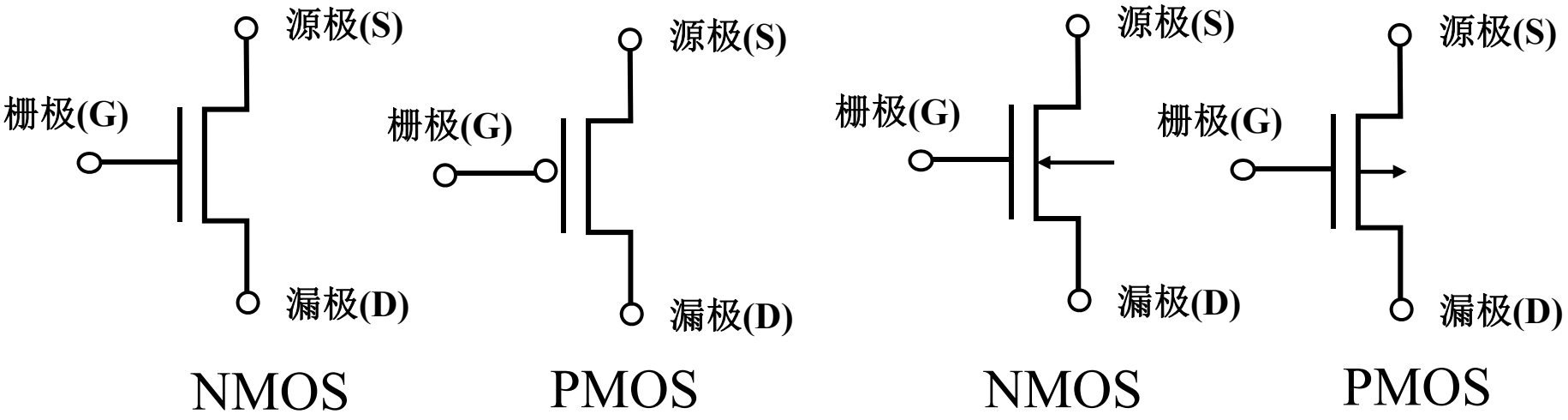
MOSFET的基本结构

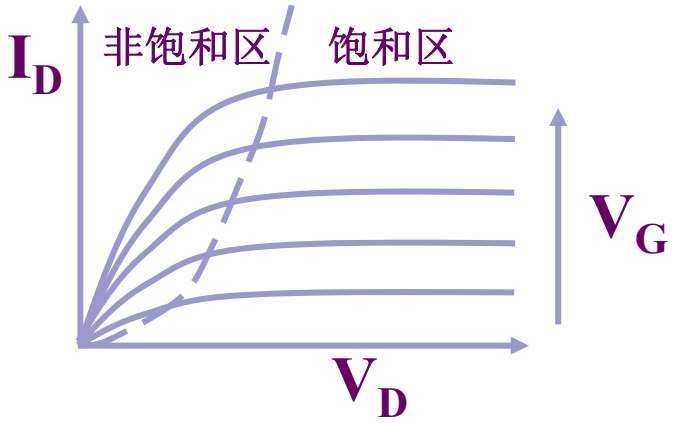
N沟MOS晶体管的基本结构



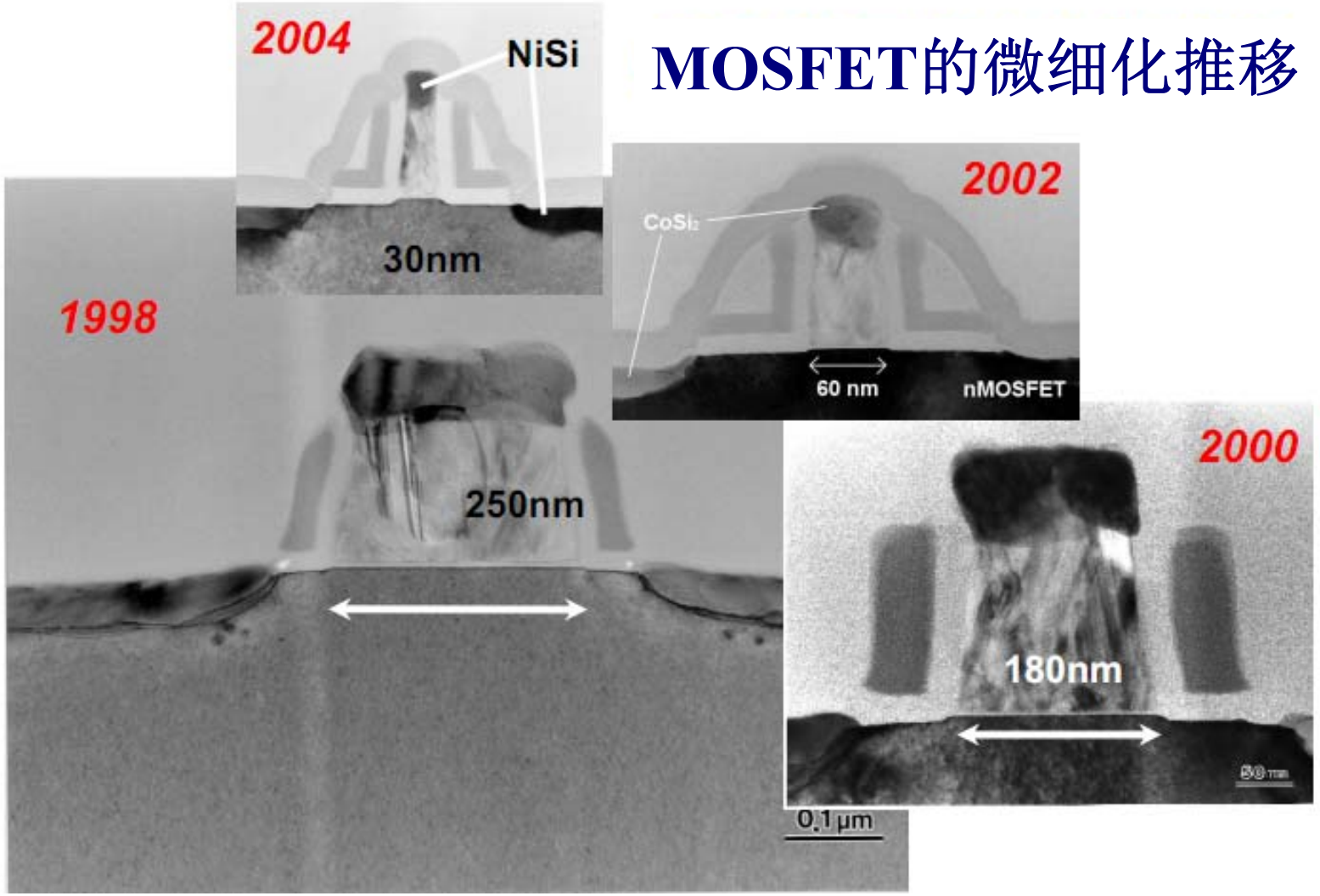
MOS晶体管的动作 ➡ MOS晶体管实质上是一种使电流时而流过，时而切断的开关

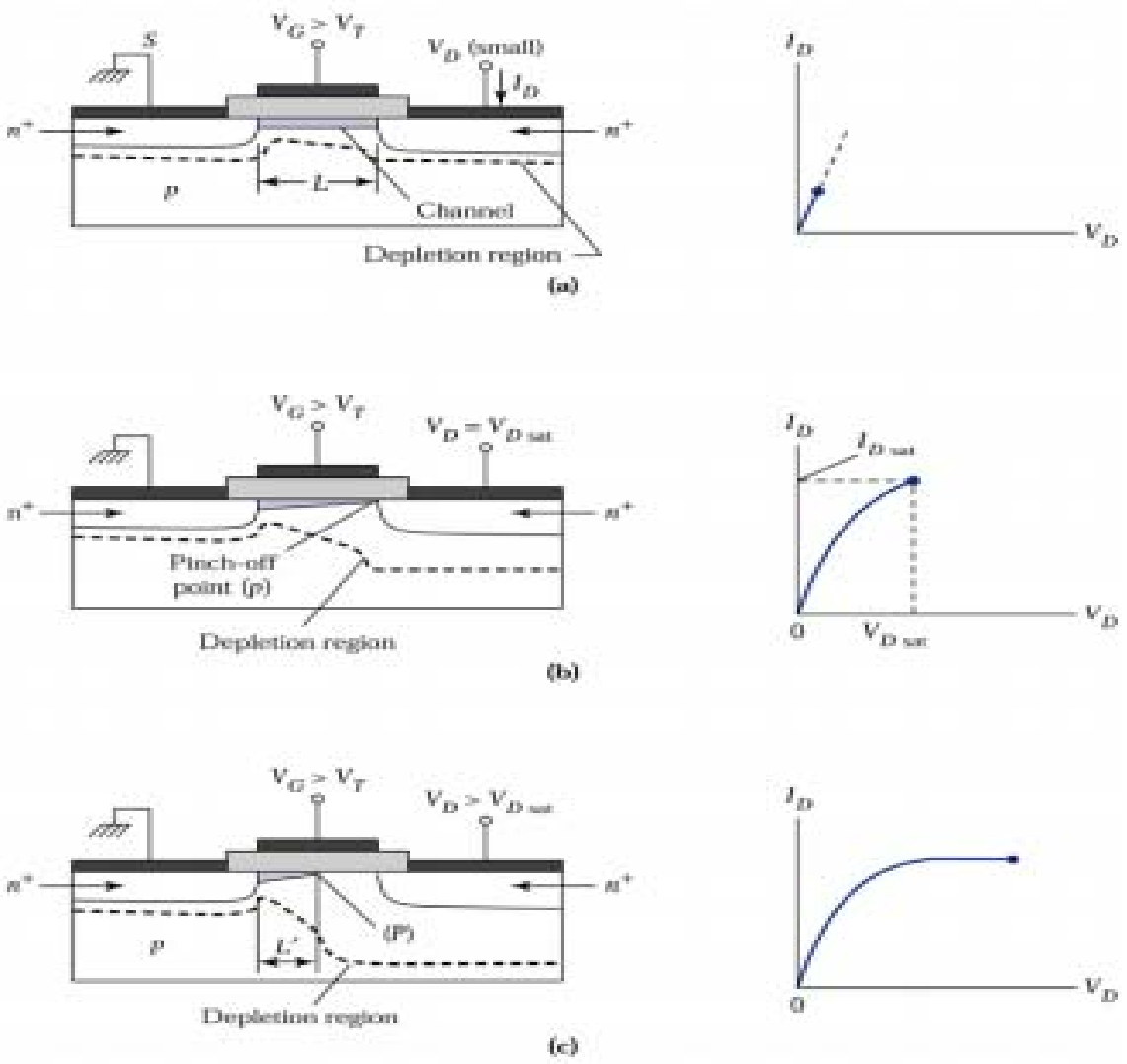
MOS晶体管的符号

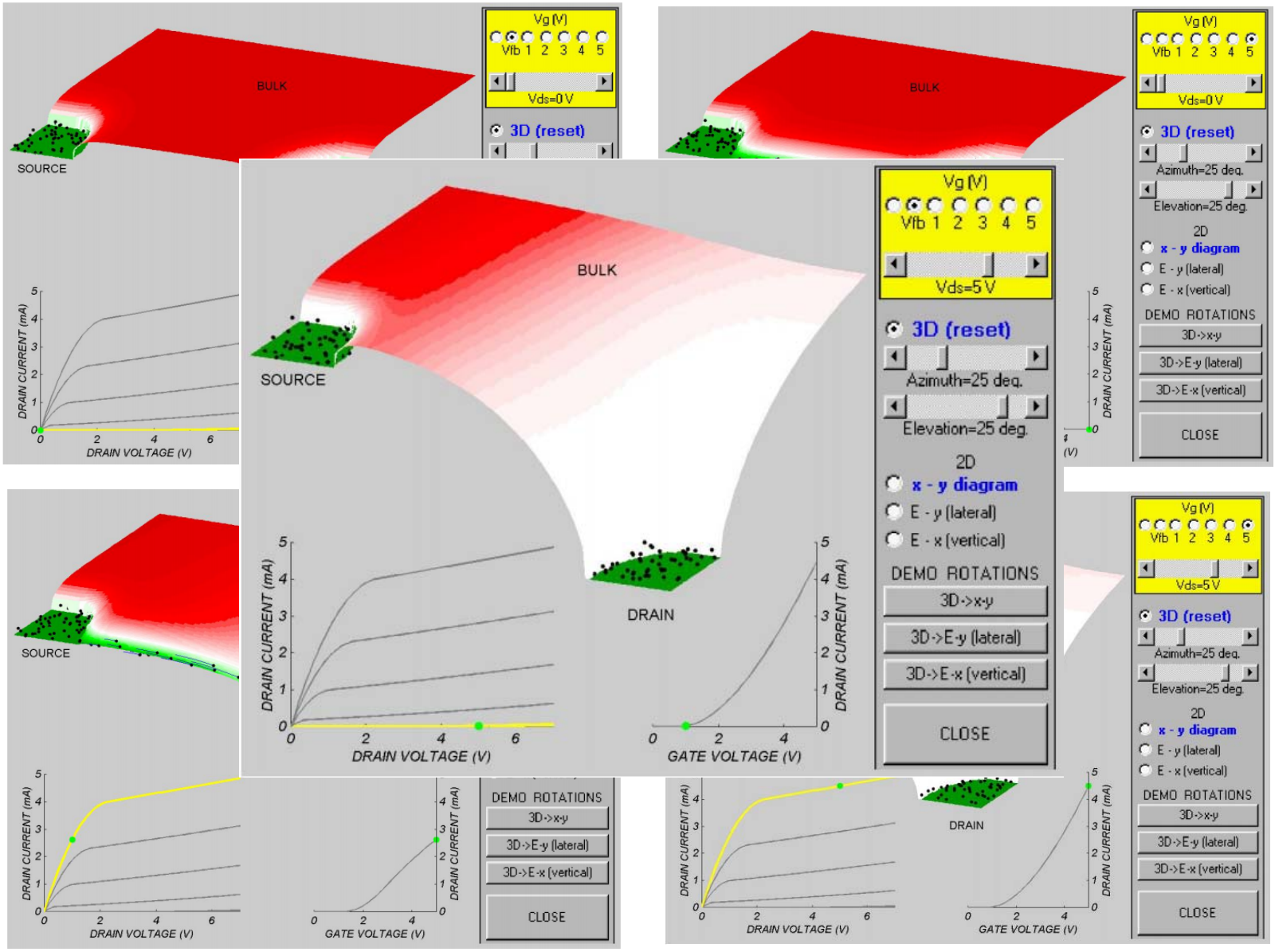

源极(S)
栅极(G)
漏极(D)
源极(S)
栅极(G)
漏极(D)
NMOS
PMOS
(a)
源极(S)
栅极(G)
漏极(D)
源极(S)
栅极(G)
漏极(D)
NMOS
PMOS
(b)


I_D
非饱和区
饱和区
V_G
V_D

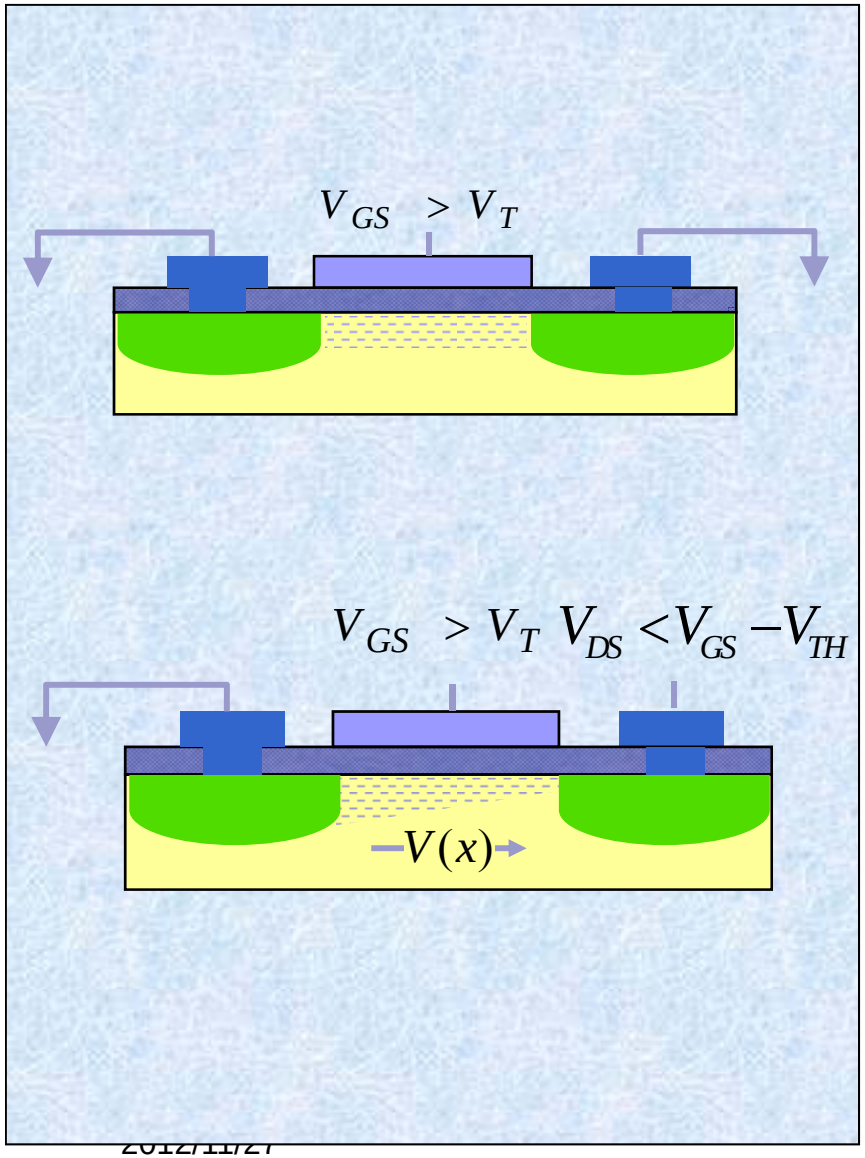
MOSFET的微细化推移




$V_G > V_T$
S
V_D (small)
I_D
n^+
n^+
p
L
Channel
Depletion region
(a)
I_D
V_D
$V_G > V_T$
$V_D = V_{D\,sat}$
n^+
n^+
Pinch-off
point (p)
Depletion region
(b)
I_D
$I_{D\,sat}$
0
$V_{D\,sat}$
V_D
$V_G > V_T$
$V_D > V_{D\,sat}$
n^+
n^+
(P)
p
L'
Depletion region
(c)
I_D
0
V_D


BULK
SOURCE
DRAIN
Vg (V)
Vfb 1 2 3 4 5
Vds=0 V
Vds=5 V
3D (reset)
Azimuth=25 deg.
Elevation=25 deg.
2D
x - y diagram
E - y (lateral)
E - x (vertical)
DEMO ROTATIONS
3D->x-y
3D->E-y (lateral)
3D->E-x (vertical)
CLOSE
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
GATE VOLTAGE (V)

非饱和区的电流方程



$$Q = C_G(V_{GS} - V_T) = \frac{\varepsilon WL}{t_{ox}}(V_{GS} - V_T)$$

$$Q(x) = WC_{ox}[V_{GS} - V_{TH} - V(x)]_{V(0)=0, V(L)=V_{DS}}$$

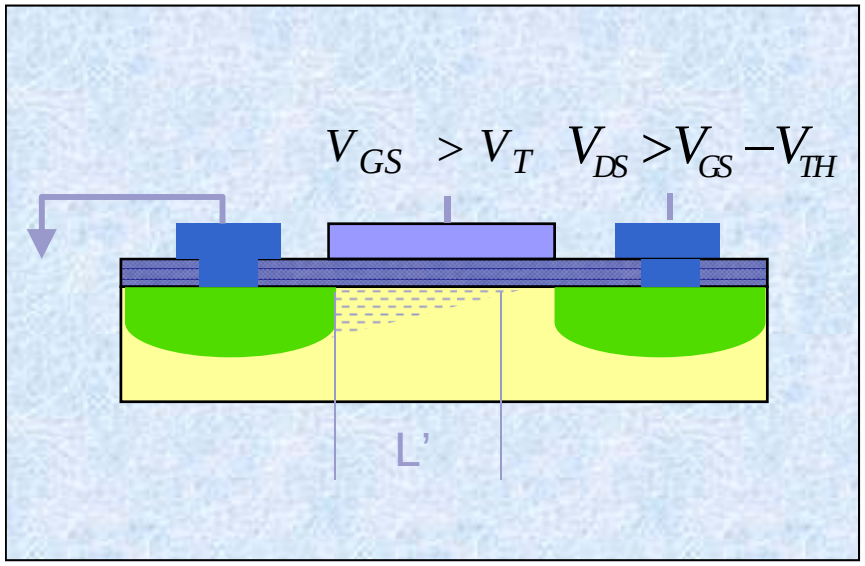
$$I = -Q(x)v, \; v = \mu E = \mu \frac{dV}{dx}$$

$$I_{DS} = WC_{ox}[V_{GS} - V_{TH} - V(x)]\mu \frac{dV}{dx}$$

$$\int_{x=0}^{L} I_{DS}\,dx = \int_{V=0}^{V=V_{DS}} WC_{ox}\mu[V_{GS} - V_{TH} - V(x)]\,dV$$

$$I_{DS} = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{\,2}]$$

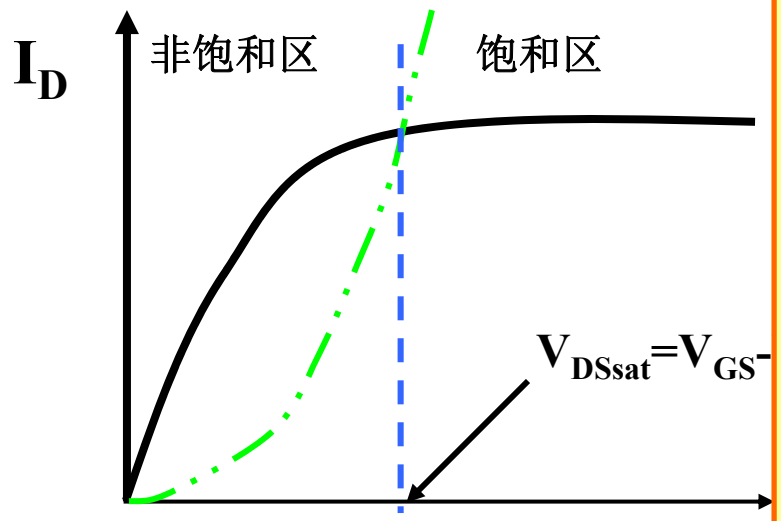
饱和区的电流方程



$$\int_{x=0}^{L'} I_{DS}\,dx = \int_{V=0}^{V_{GS}-V_{TH}} WC_{ox}\mu[V_{GS} - V_{TH} - V(x)]dV$$

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

沟道长度调制效应

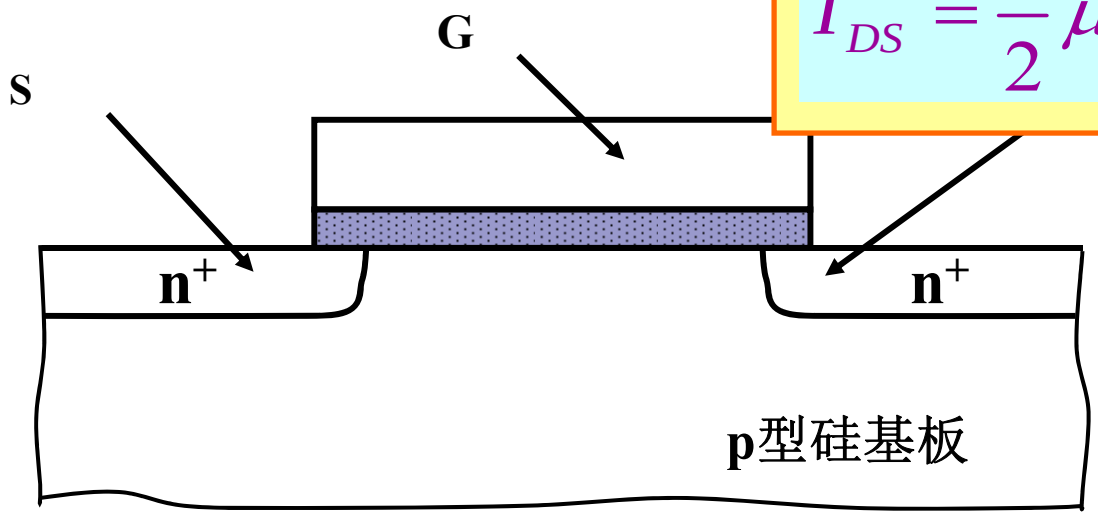


非饱和区的电流方程:

$$I_{DS} = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^{2}]$$

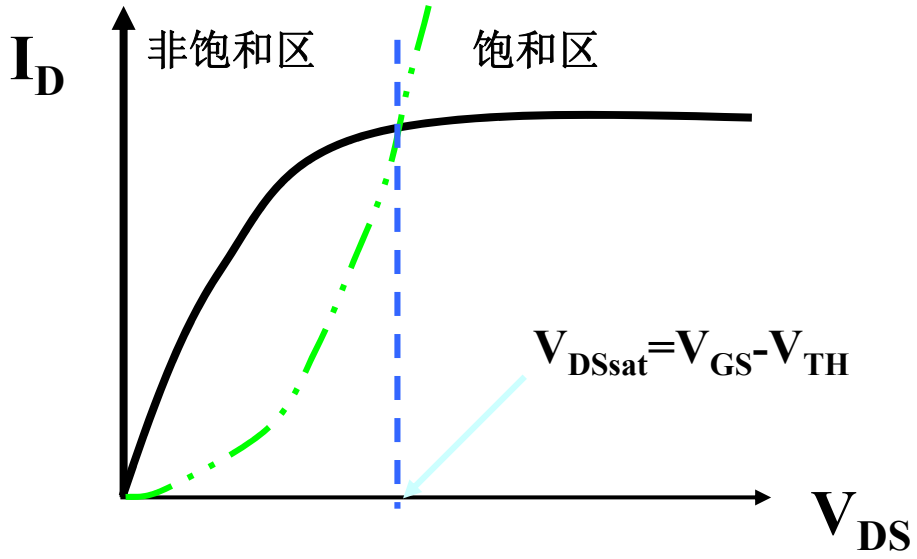
饱和区的电流方程:

$$I_{DS} = \frac{1}{2}\mu C_{ox} \frac{W}{L'}(V_{GS} - V_{TH})^2$$



记住

NMOS晶体管的I/V特性-1

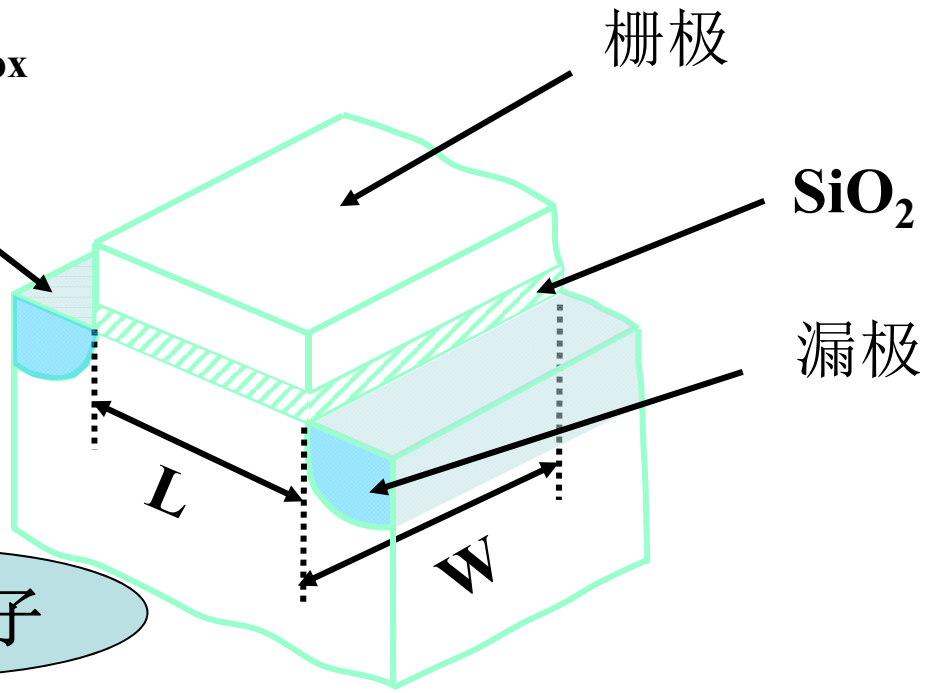


$$I_D \begin{cases} I_{DS} = \mu C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] & (0<V_{DS}<V_{GS}-V_{TH}) \\ I_{DS} = \frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 & (0< V_{GS}-V_{TH} < V_{DS}) \end{cases}$$

常令 $K_n'=\mu_n C_{ox}$，$K_p'=\mu_p C_{ox}$

$$K_n=\frac{1}{2}\frac{\mu_n C_{ox} W}{L}$$

$$K_p=\frac{1}{2}\frac{\mu_p C_{ox} W}{L}$$



$\frac{\mu_n C_{ox} W}{L}$

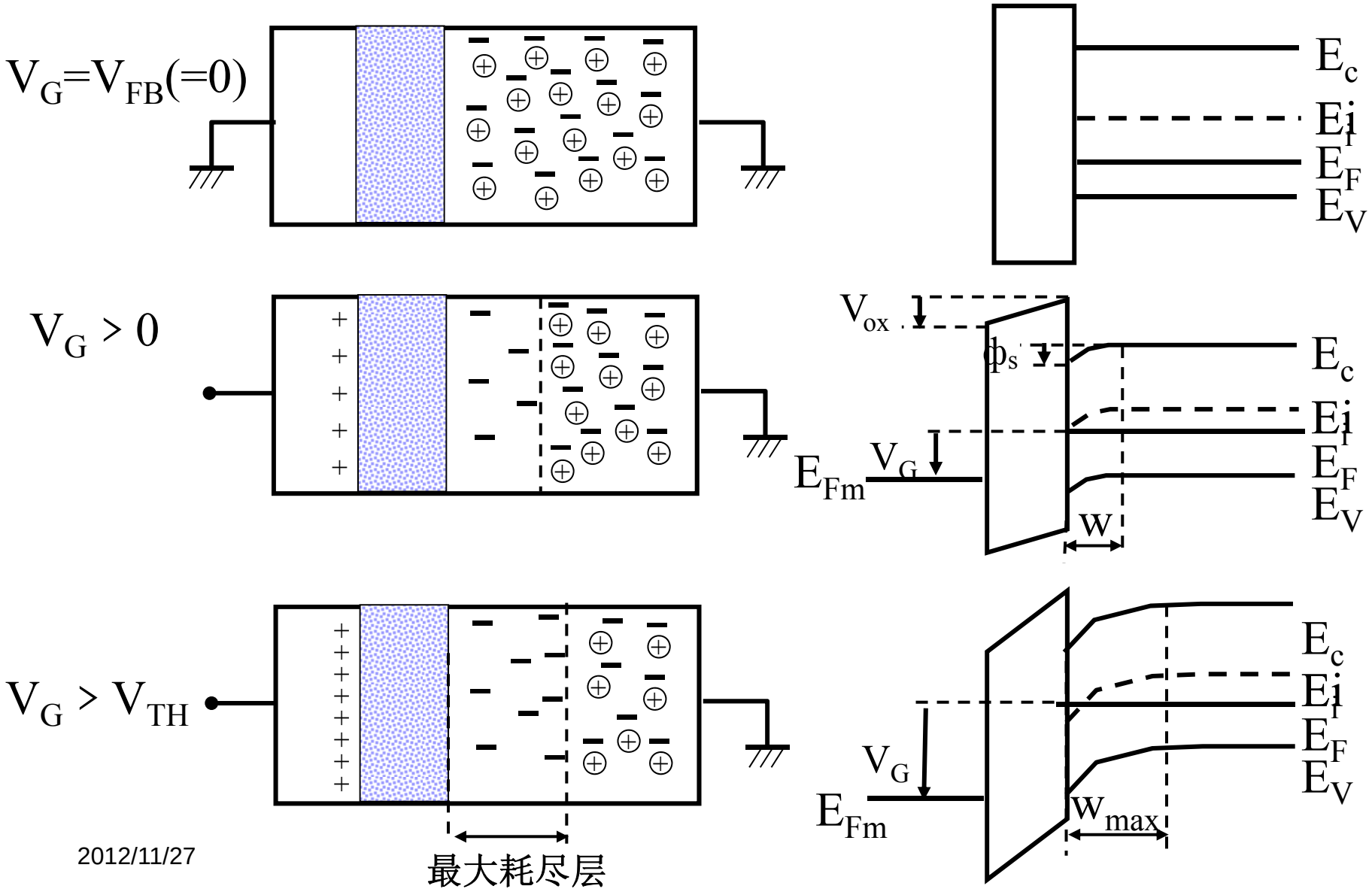
导电因子

μ_n ： 为Si中电子的迁移率
C_{ox}： 为栅极单位电容量
W ： 为沟道宽
L ： 为沟道长

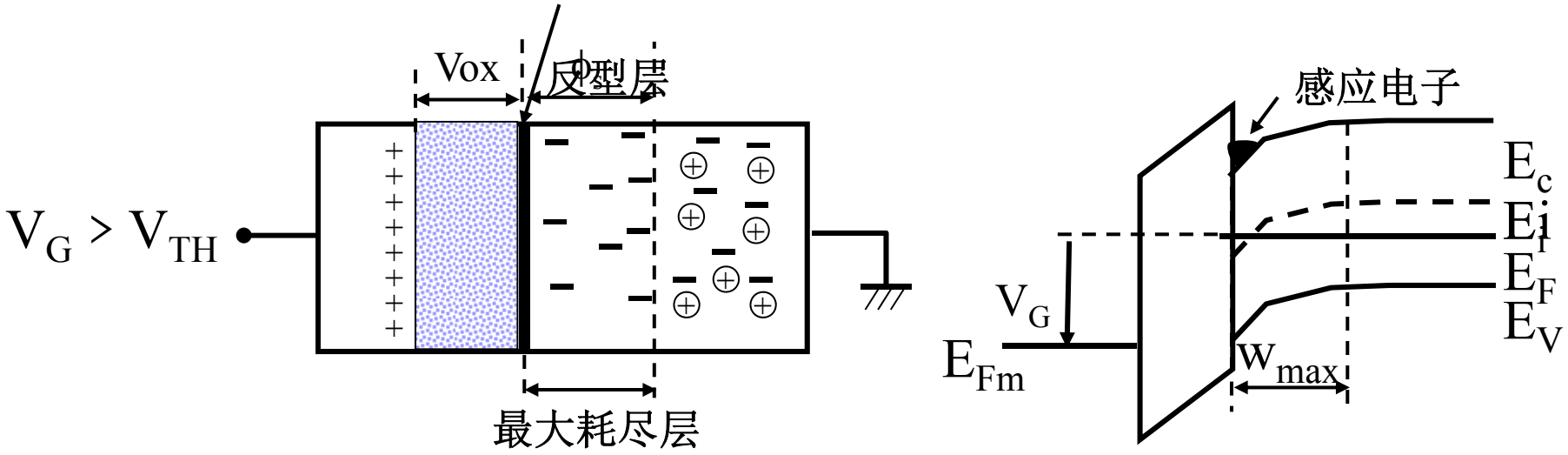
C_{ox}

$C_{ox}=\varepsilon_{ox}/t_{OX}$

MOS晶体管的阈值电压-1



MOS晶体管的阈值电压-2



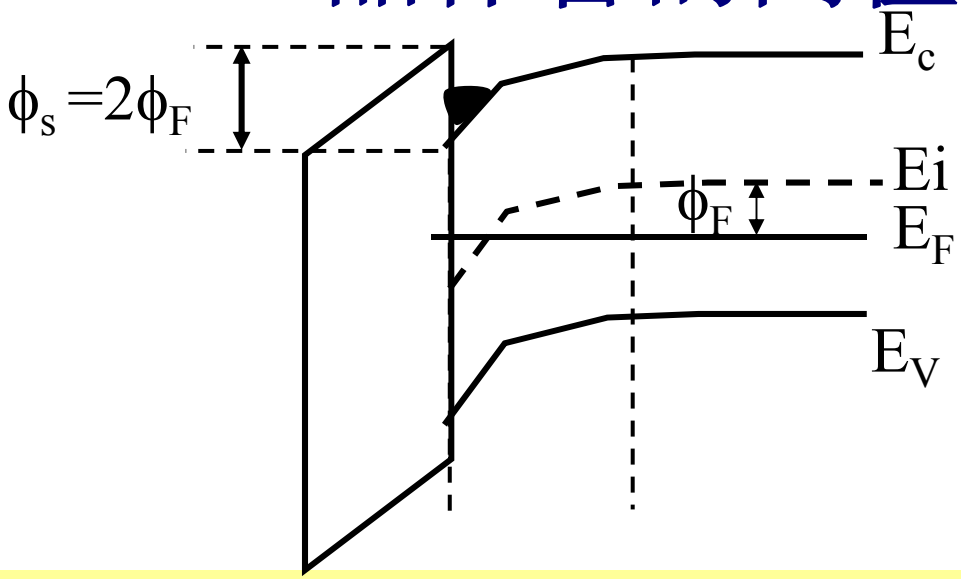
$$V_G = W = \sqrt{\frac{2\varepsilon_0\varepsilon_s\phi_s}{qN_A}} \qquad C_{OX} = \frac{\varepsilon_0\varepsilon_s}{t_{ox}}$$

$$Q_S = -C_{OX}V_{OX} \quad \Leftrightarrow \quad Q_D = -qN_AW$$

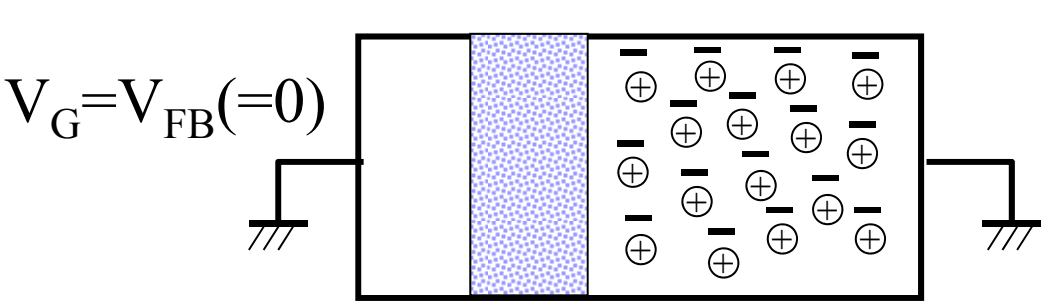
$$V_{OX} = -\frac{Q_S}{C_{OX}} = \frac{qN_AW}{C_{OX}} = \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A\phi_s}$$

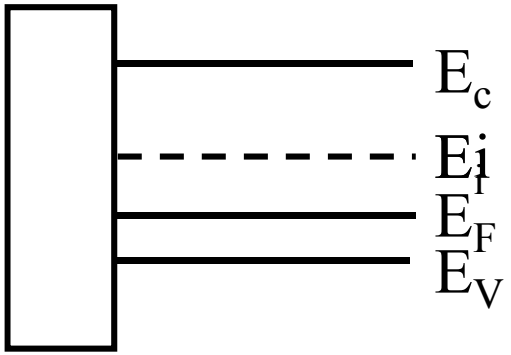
$$V_G = \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A\phi_s} + \phi_s$$

MOS晶体管的阈值电压-3



$$V_{TH} = \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A(2\phi_F)} + 2\phi_F = -\frac{Q_D}{C_{OX}} + 2\phi_F$$





$V_{FB} \neq 0$

$$V_{TH} = V_{FB} - \frac{Q_D}{C_{OX}} + 2\phi_F$$

MOS晶体管的阈值电压-4

$$V_{TH} = V_{FB} - \frac{Q_D}{C_{OX}} + 2\phi_F$$

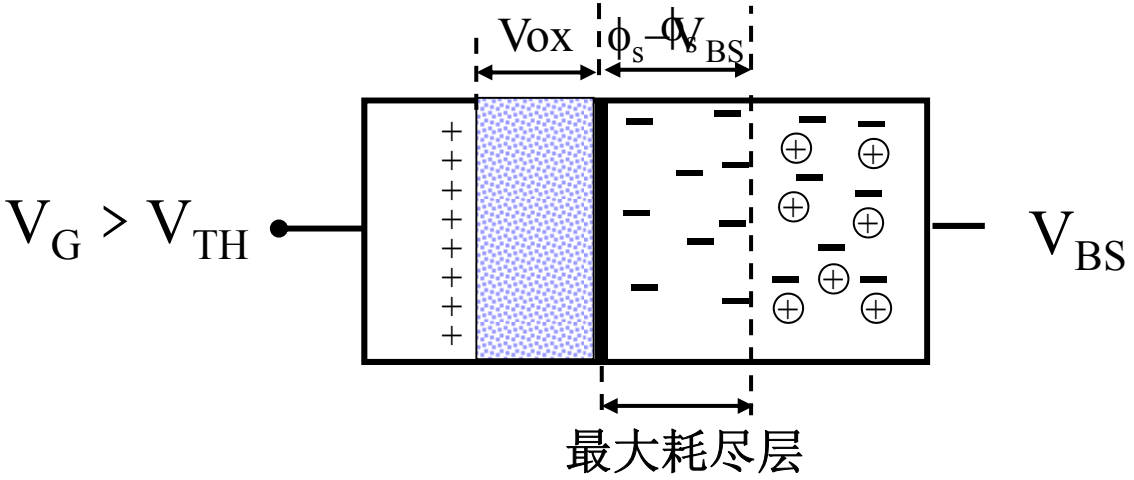
V_{FB} = 金属/半导体功函数的差 + 二氧化硅中的固定正电 荷

$$V_{FB} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}}$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \frac{Q_D}{C_{OX}} + 2\phi_F$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A(2\phi_F)} + 2\phi_F$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \gamma\sqrt{(2\phi_F)} + 2\phi_F \qquad \gamma = \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A}$$



$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \gamma\sqrt{(2\phi_F)} + 2\phi_F$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \gamma\sqrt{(2\phi_F - V_{BS})} + 2\phi_F$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \gamma\sqrt{(2\phi_F - V_{BS})} + 2\phi_F \qquad \gamma = \frac{1}{C_{OX}}\sqrt{2\varepsilon_0\varepsilon_s qN_A}$$

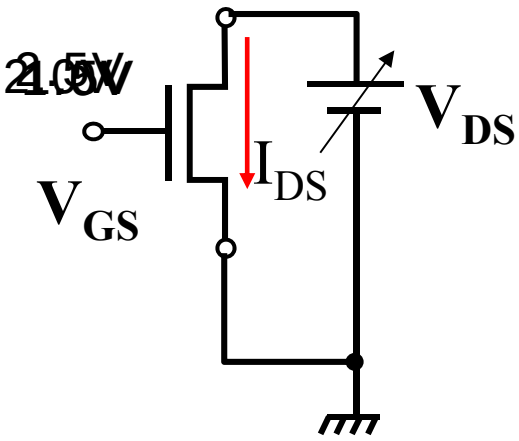
功函数差　SiO,表面电荷　衬底偏压　费米势

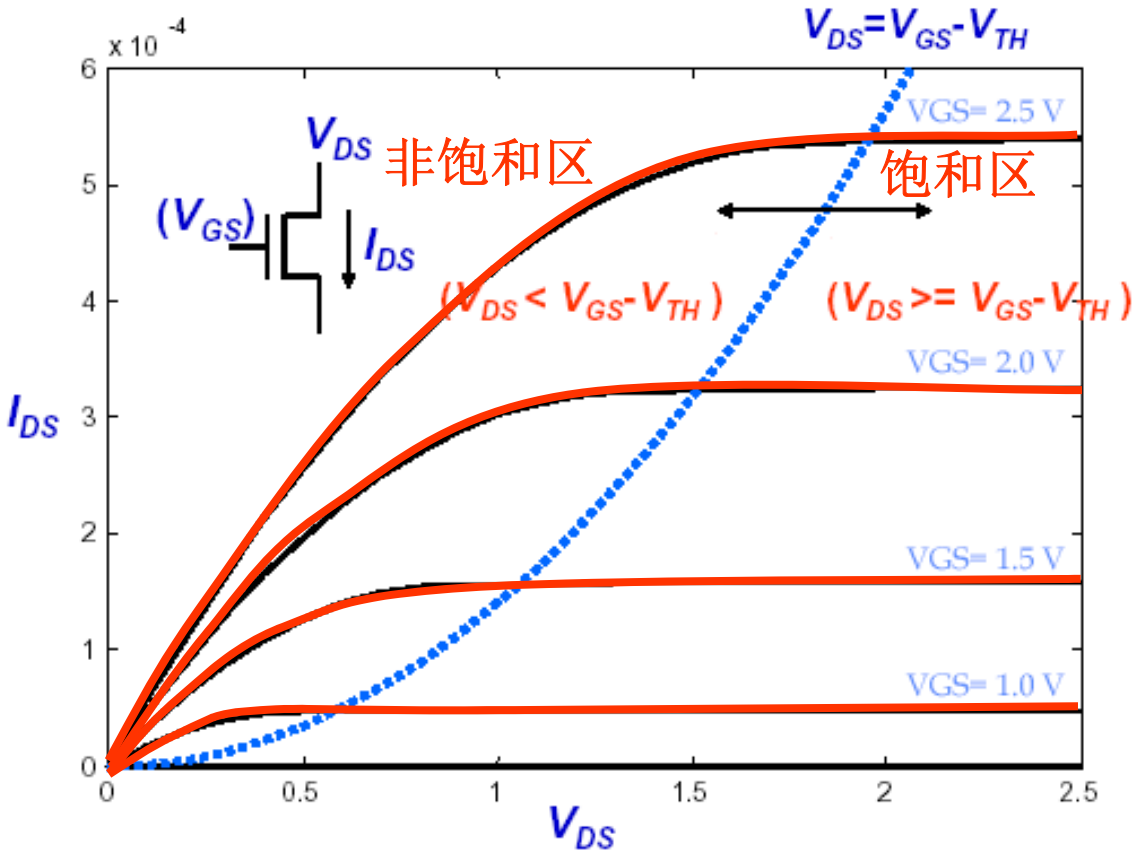
$$I_D \begin{cases} I_{DS} = \mu C_{ox}\frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] & (0<V_{DS}<V_{GS}-V_{TH}) \\ I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 & (0< V_{GS}-V_{TH} < V_{DS}) \end{cases}$$

影响MOS晶体管特性的几个重要参数

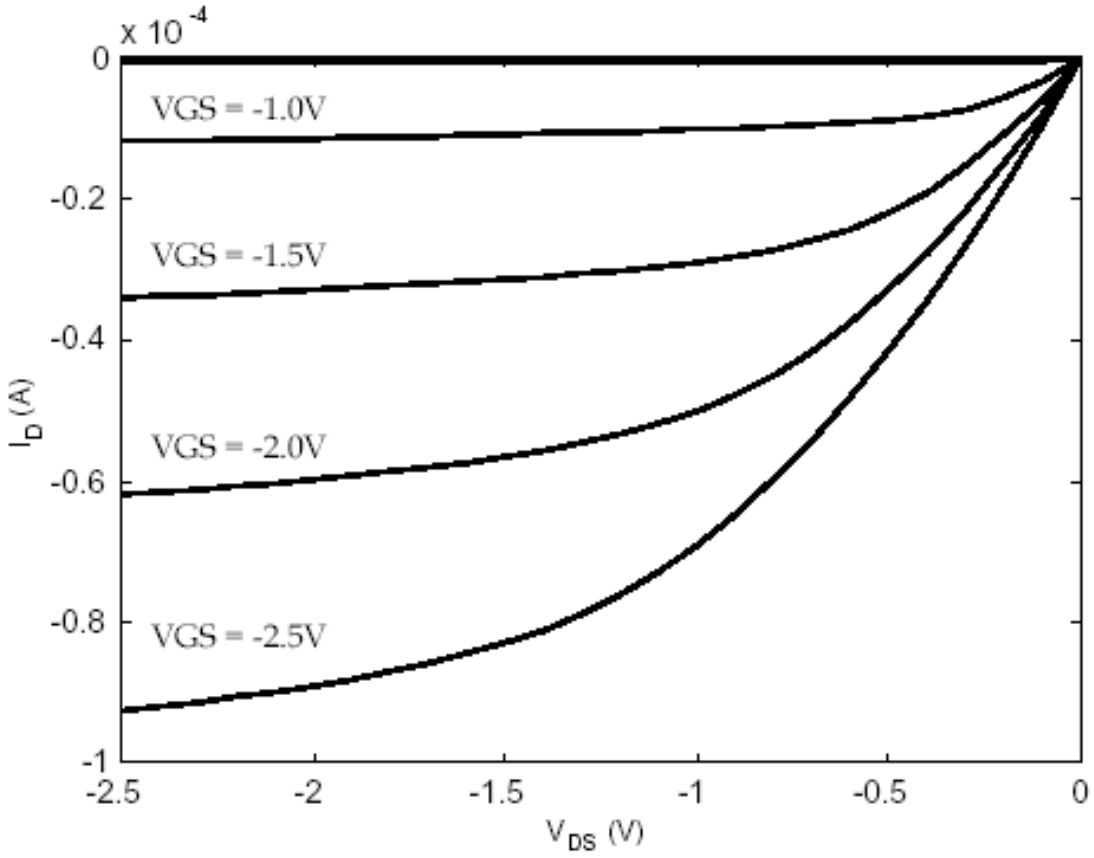
- MOS晶体管的宽长比（W/L)
- MOS晶体管的开启电压V_{TH}
  - 栅极氧化膜的厚度t_{ox}
  - 沟道的掺杂浓度（N_A)
  - 衬底偏压（V_{BS})

NMOS的I_{DS}-V_{DS}特性 (沟道长>1μm)





PMOS的I_{DS}-V_{DS}特性 (沟道长>1μm)



MOS管的电流解析方程（L〉1μm)

$$I_D \begin{cases} I_{DS} = K_n[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] & (0<V_{DS}<V_{GS}-V_{TH}) \\ I_{DS} = K_n(V_{GS} - V_{TH})^2(1+\lambda V_{DS}) & (0< V_{GS}-V_{TH} < V_{DS}) \end{cases}$$

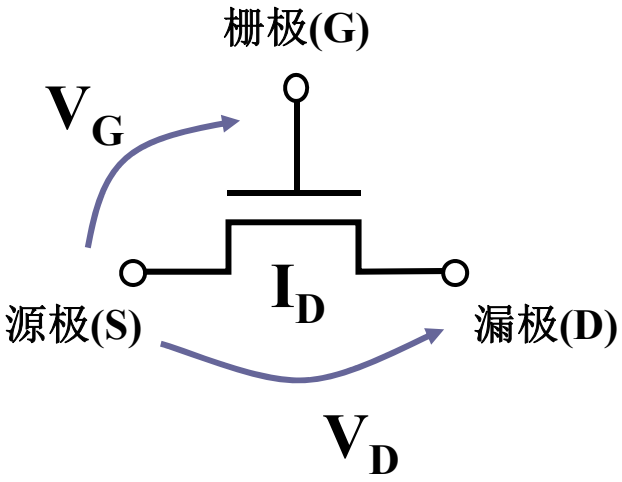
$$K_n = \frac{1}{2}\frac{\mu_n C_{ox} W}{L}$$ 工艺参数

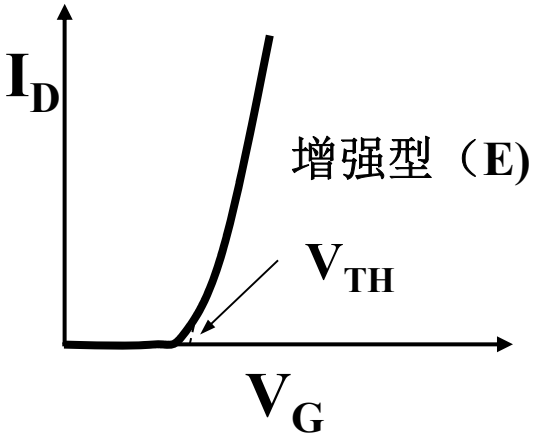
V_{TH} — 阈值电压

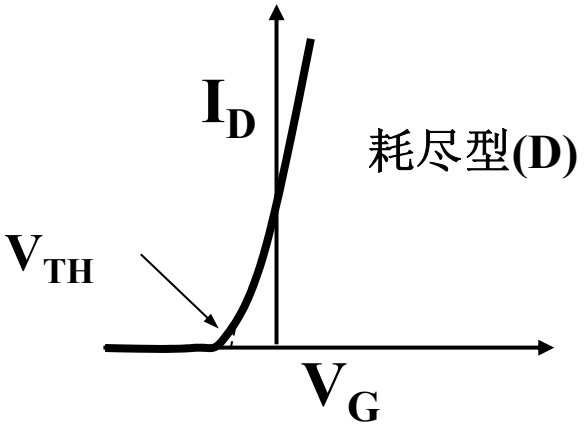
λ — 沟道长度调制系数

NMOS晶体管的I/V特性-2（转移特性）

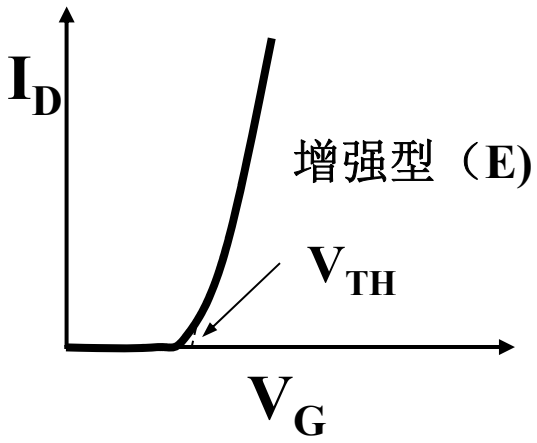
nMOS晶体管的I-V特性

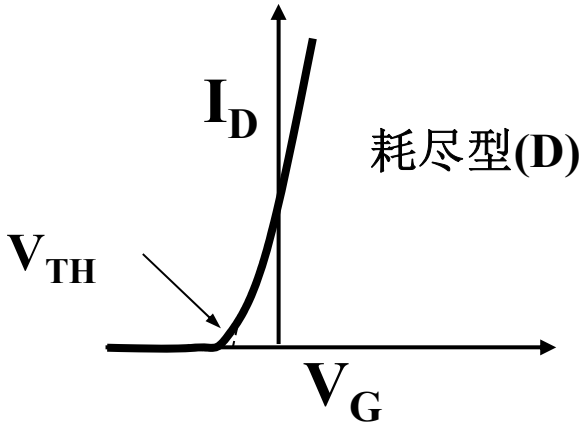


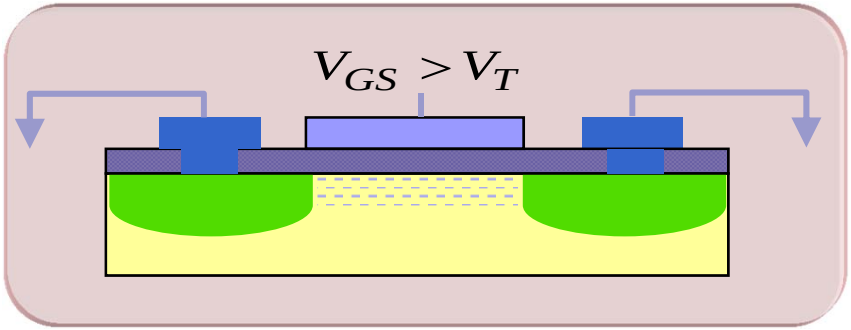


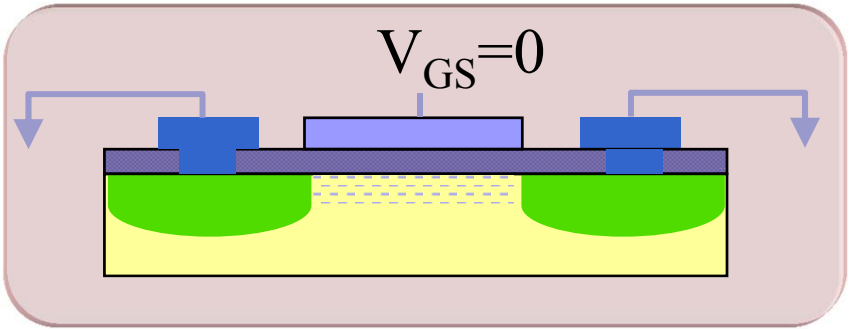


NMOS的I_D-V_G特性(转移特性)





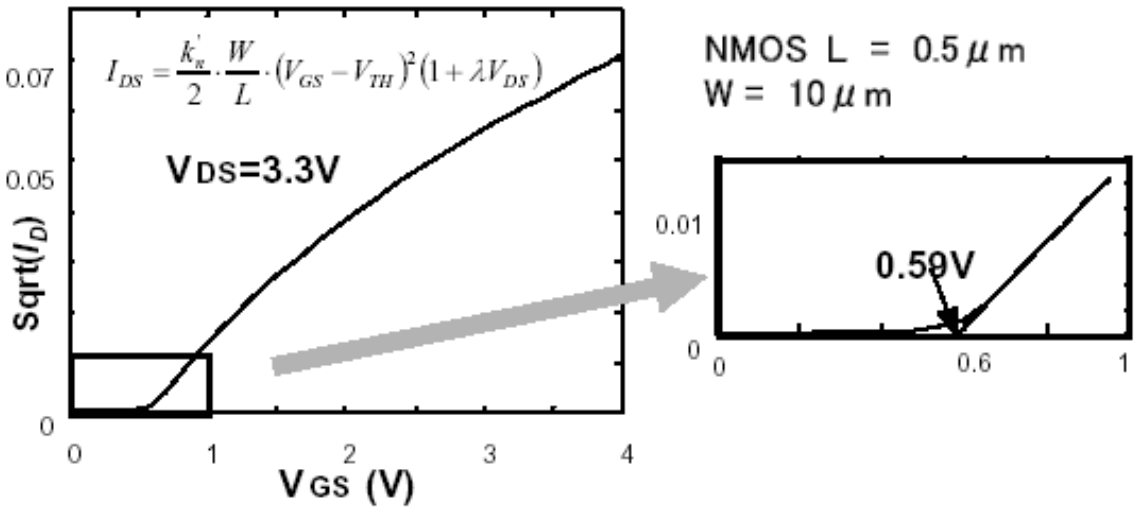




阈值电压的定义

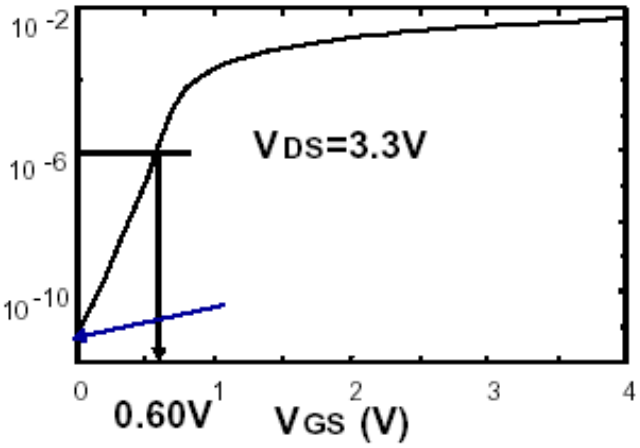
饱和区外插V_{TH}

在晶体管的漏源极加上接近电源VDD的电压，画出V_{GS}-I_{DS}的关系曲线，找出该曲线的最大斜率，此斜率与X轴的交点定义为阈值电压。

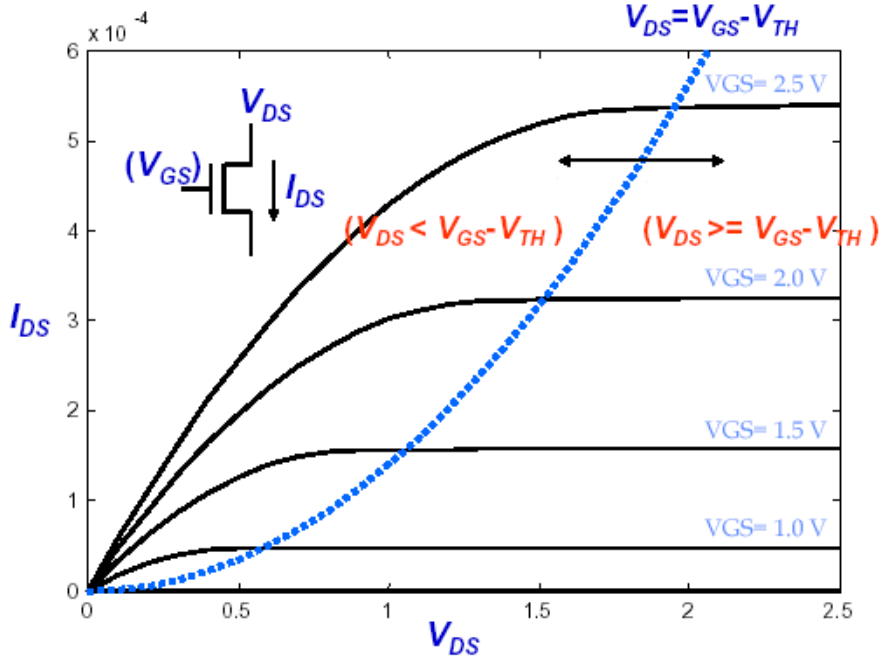


以漏电流为依据定义V_{TH}

在晶体管的漏源极加上接近电源VDD的电压，画出V_{GS}-Log(I_{DS})的关系曲线，从该曲线中找出电流为1微安时所对应的V_{GS}定义为阈值电压。



MOS管的跨导g_m（饱和区）

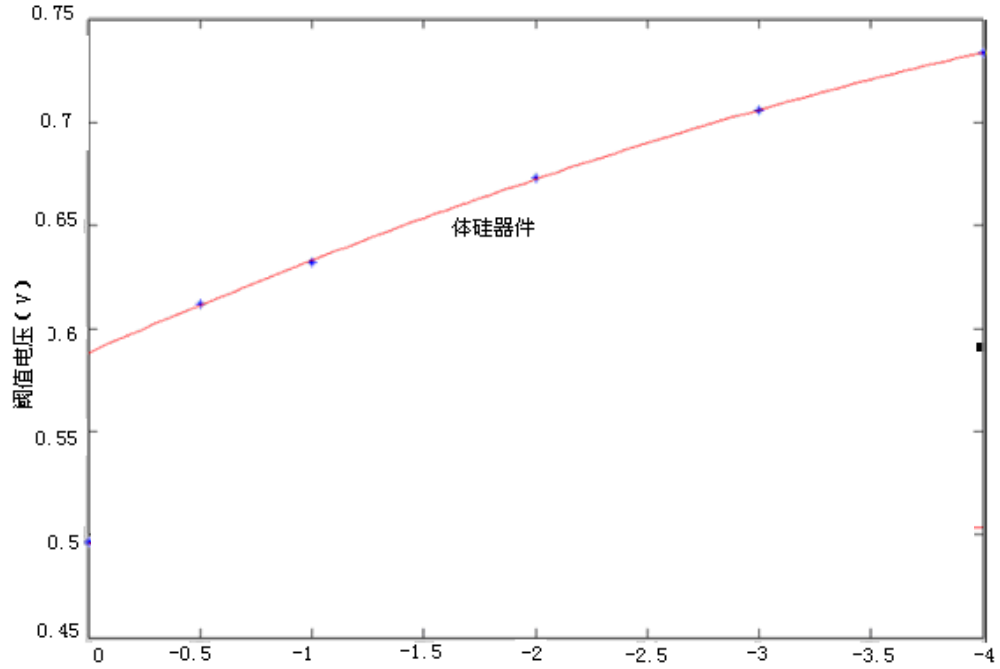


$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{常数}} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$$

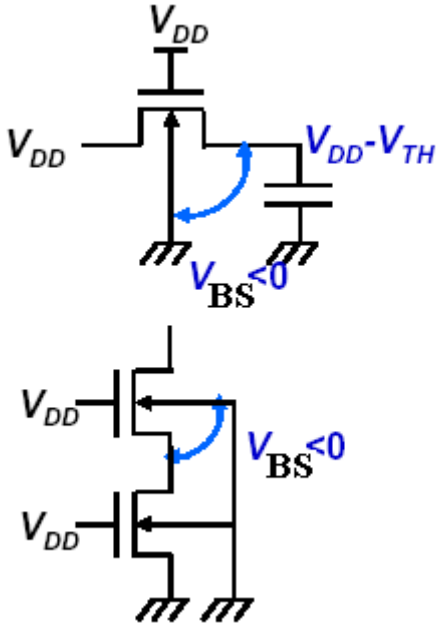
表征电压转换电流的能力

衬底偏压效应

- 通常衬底偏压V_{BS}=0, 即NMOS的衬底和源都接地，PMOS衬底和源都接电源。
- 衬底偏压V_{BS}<0时，阈值电压增大。



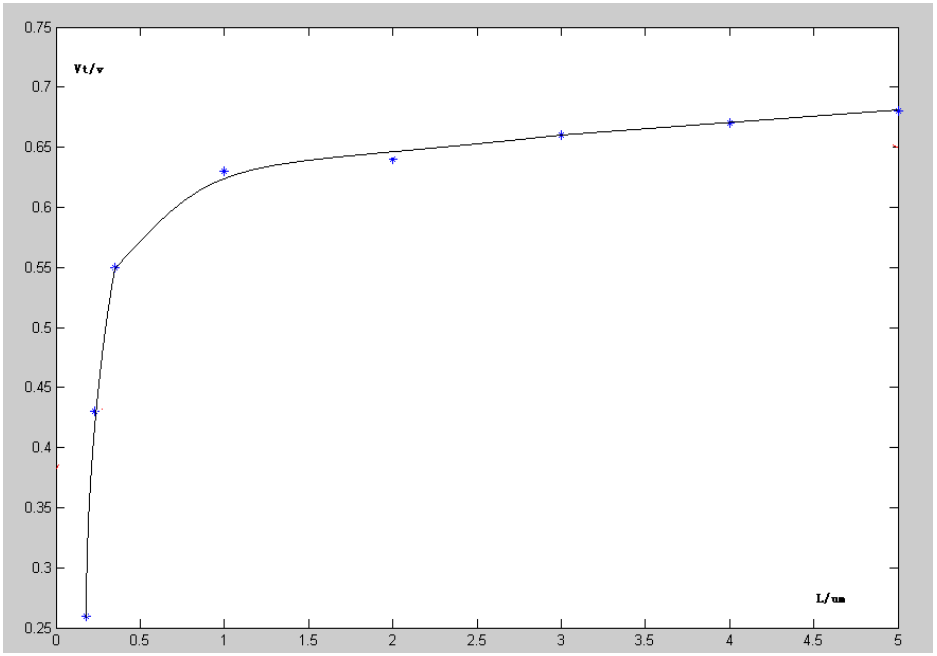
V_{BS}(V)

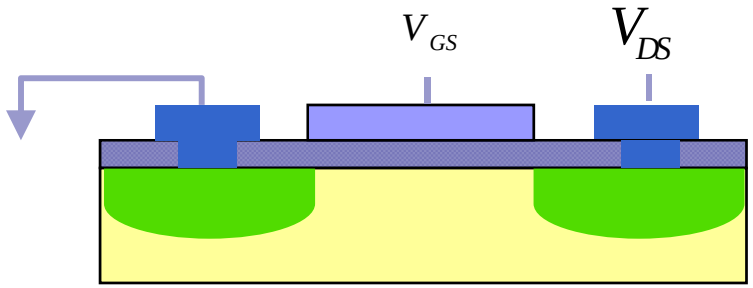


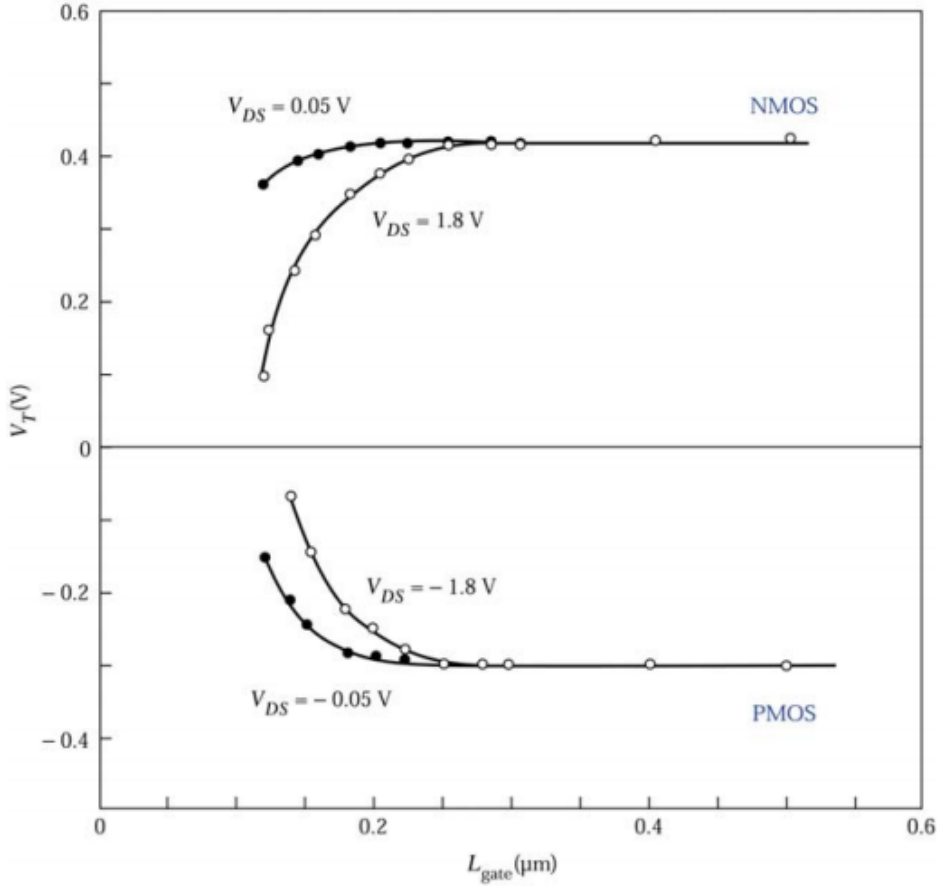
MOS管短沟道效应

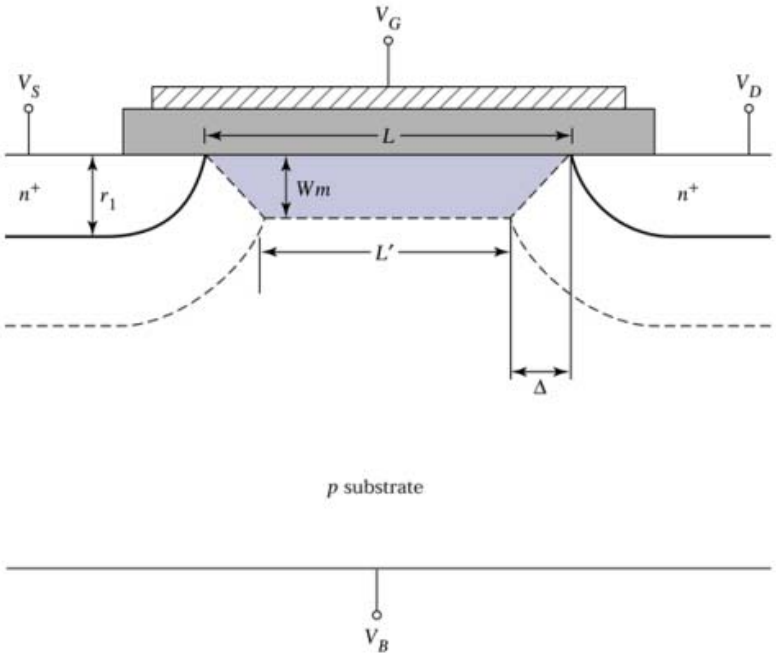
- I_{DS} 正比于 W/L，L要尽可能小

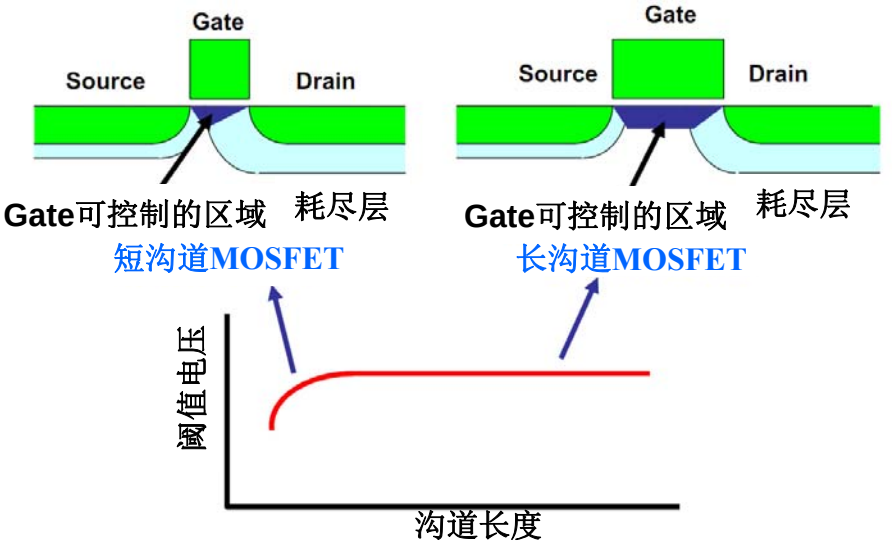
- 当沟道长度变短到可以与源漏的耗尽层宽度相比拟时，发生短沟道效应。
- 栅下耗尽区电荷不再完全受栅控制，其中有一部分受源、漏控制，并且随着沟道长度的减小，受栅控制的耗尽区电荷不断减少，因此，只需要较少的栅电荷就可以达到反型，使阈值电压降低



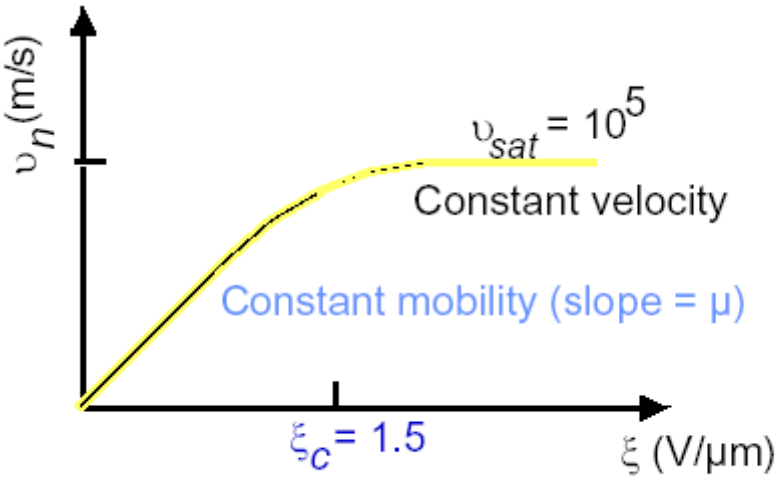



0.6
0.4
0.2
0
−0.2
−0.4
V_{DS} = 0.05 V
NMOS
V_{DS} = 1.8 V
V_{DS} = − 1.8 V
V_{DS} = − 0.05 V
PMOS
V_T(V)
0
0.2
0.4
0.6
L_{gate}(μm)

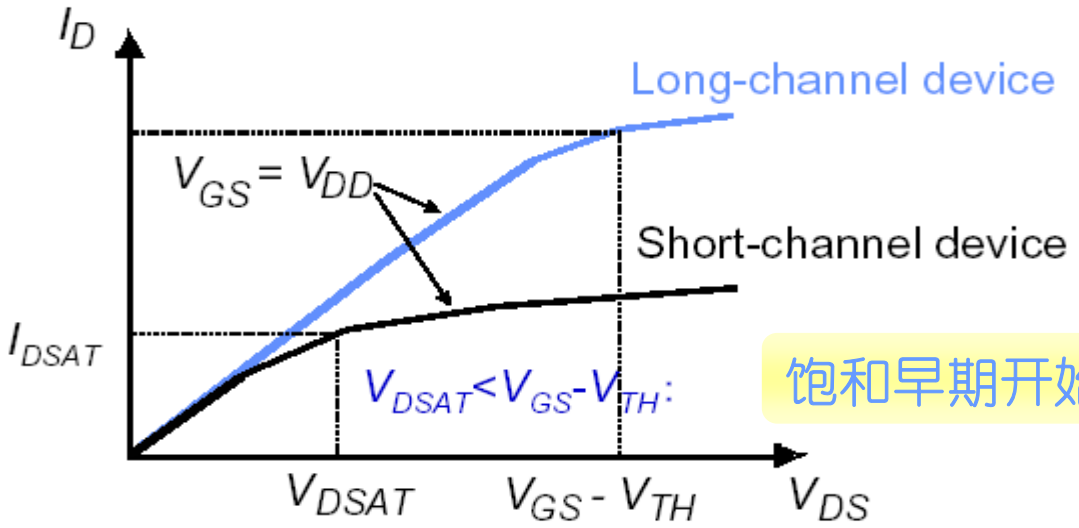

V_G
V_S
V_D
L
n^+
r_1
Wm
n^+
L′
Δ
p substrate
V_B


Gate
Source
Drain
Gate可控制的区域
耗尽层
短沟道MOSFET
Gate
Source
Drain
Gate可控制的区域
耗尽层
长沟道MOSFET
阈值电压
沟道长度

载流子的饱和速度引起的 Early Saturation



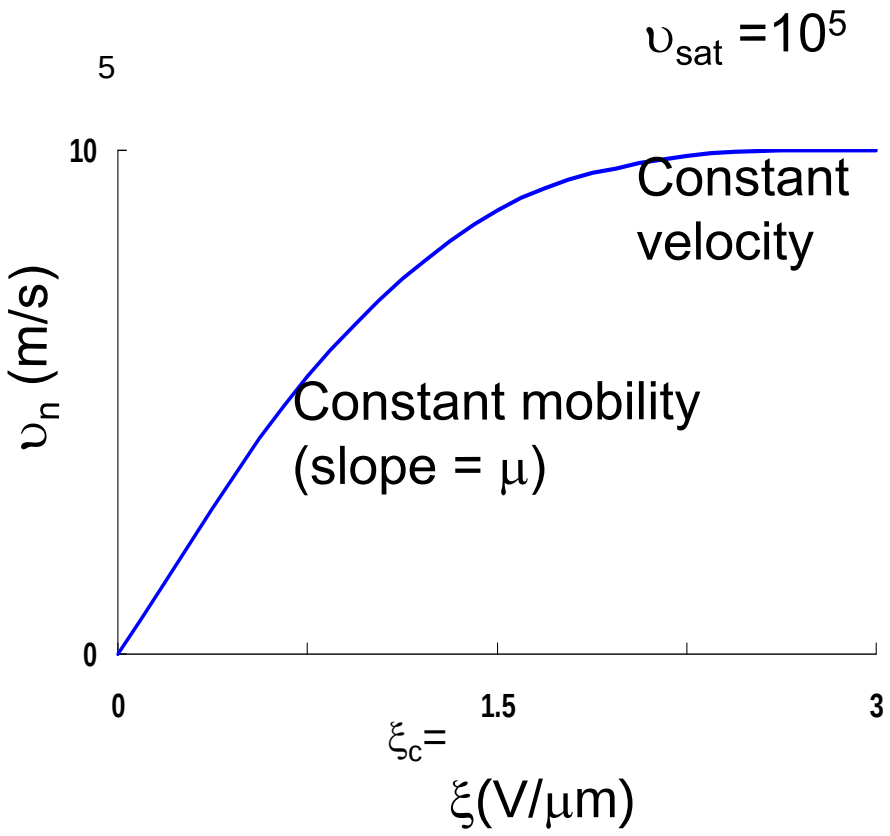
- 沟道长小于1微米时，NMOS饱和
- NMOS和PMOS的饱和速度基本相同
- PMOS不显著



饱和早期开始

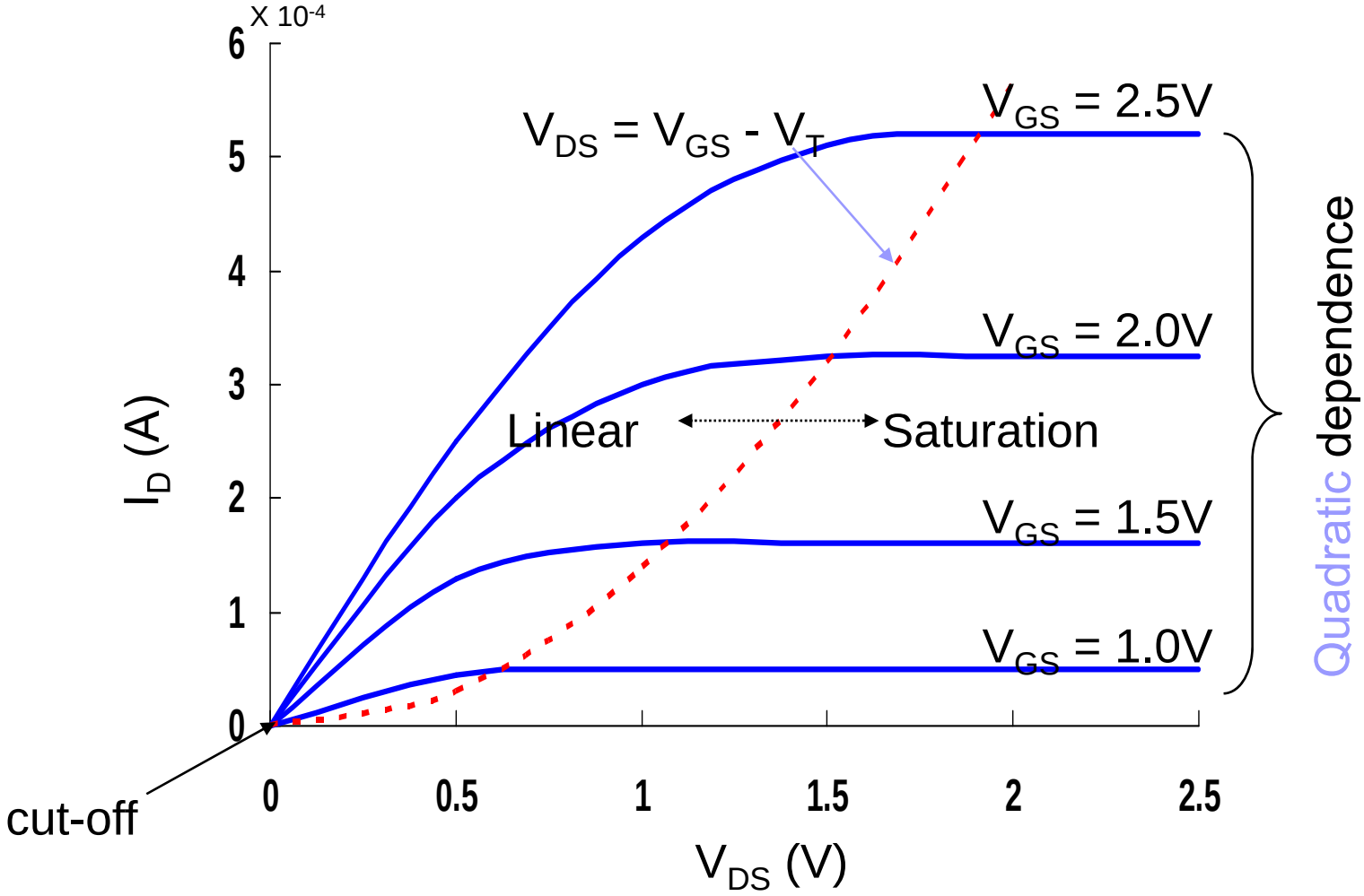
短沟道效应

- 引起短沟道效应的主要原因



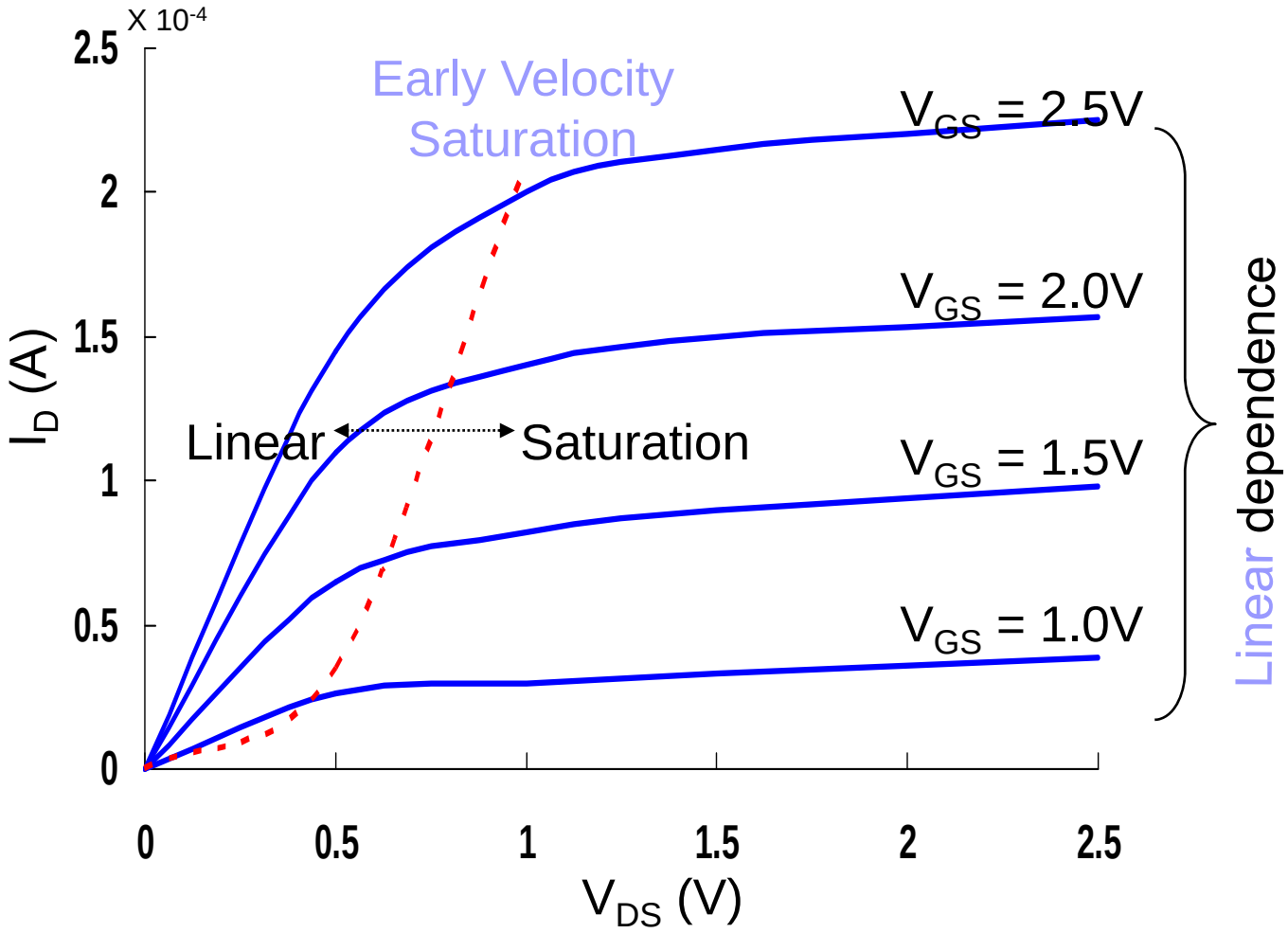
● 速度饱和 – 散射引起载流子的速度饱和 (大电场作用下载流子碰撞)

Long Channel I-V Plot (NMOS)

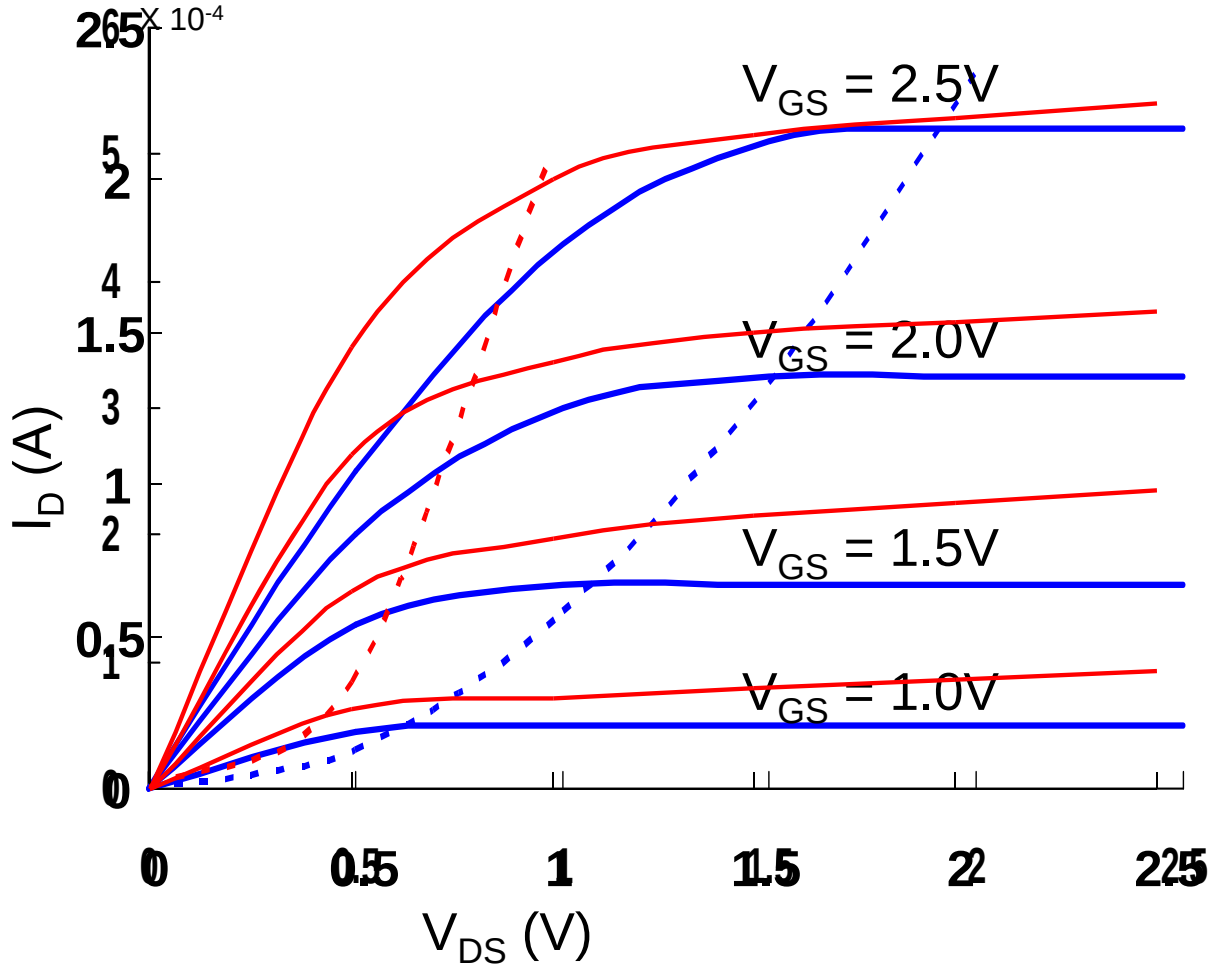


NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

Short Channel I-V Plot (NMOS)

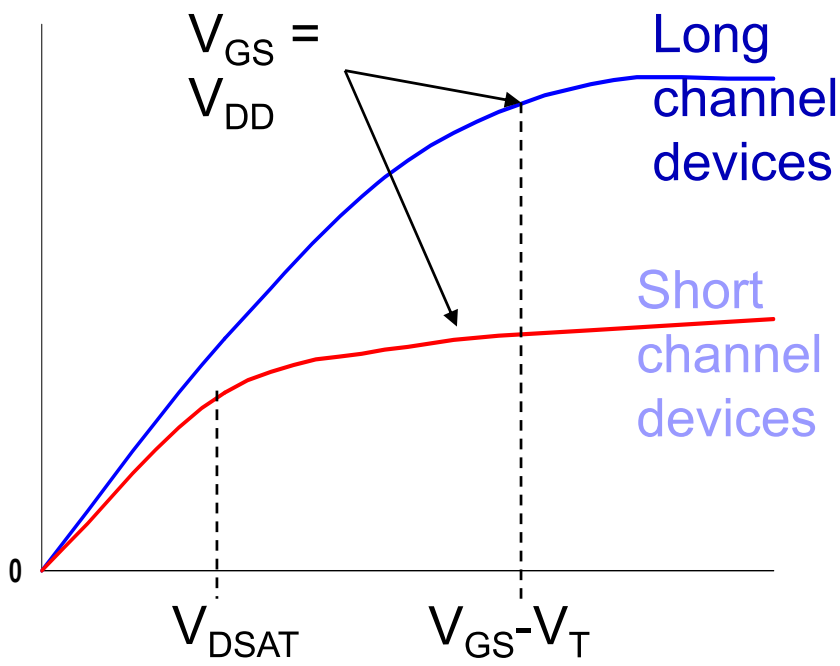


NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.4V

速度饱和



For short channel devices and large enough $V_{GS} - V_T$

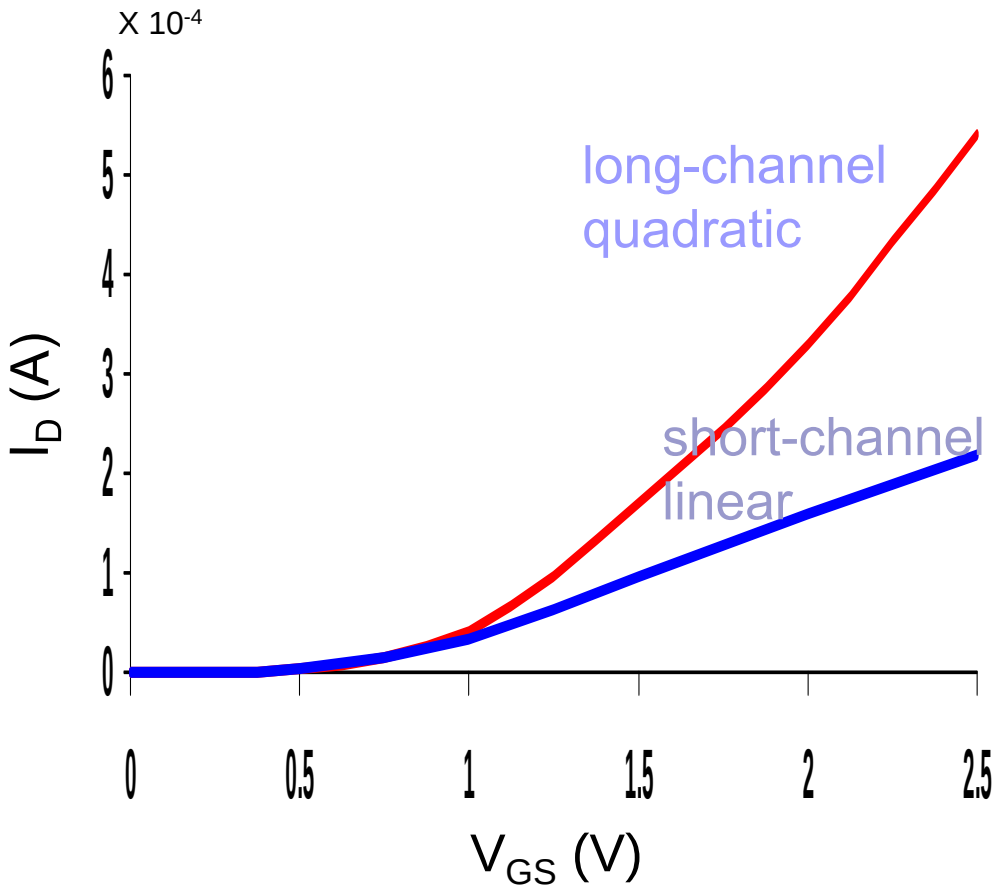
- $V_{DSAT} < V_{GS} - V_T$

晶体管进入早期饱和

V_{DS} 还没有达到 $V_{GS} - V_T$ 就已经进入饱和

I_{DSAT}与VGS成线性关系

MOS I_D-V_{GS} Characteristics



(for V_{DS} = 2.5V, W/L = 1.5)

- Linear (short-channel) versus quadratic (long-channel) dependence of I_D on V_{GS} in saturation
- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of V_{DS} resulting in a substantial drop in current drive

速度饱和时电压-电流之间的关系

For short channel devices

- Linear: When $V_{DS} \leq V_{GS} - V_T$

$$I_D = \kappa(V_{DS})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

where

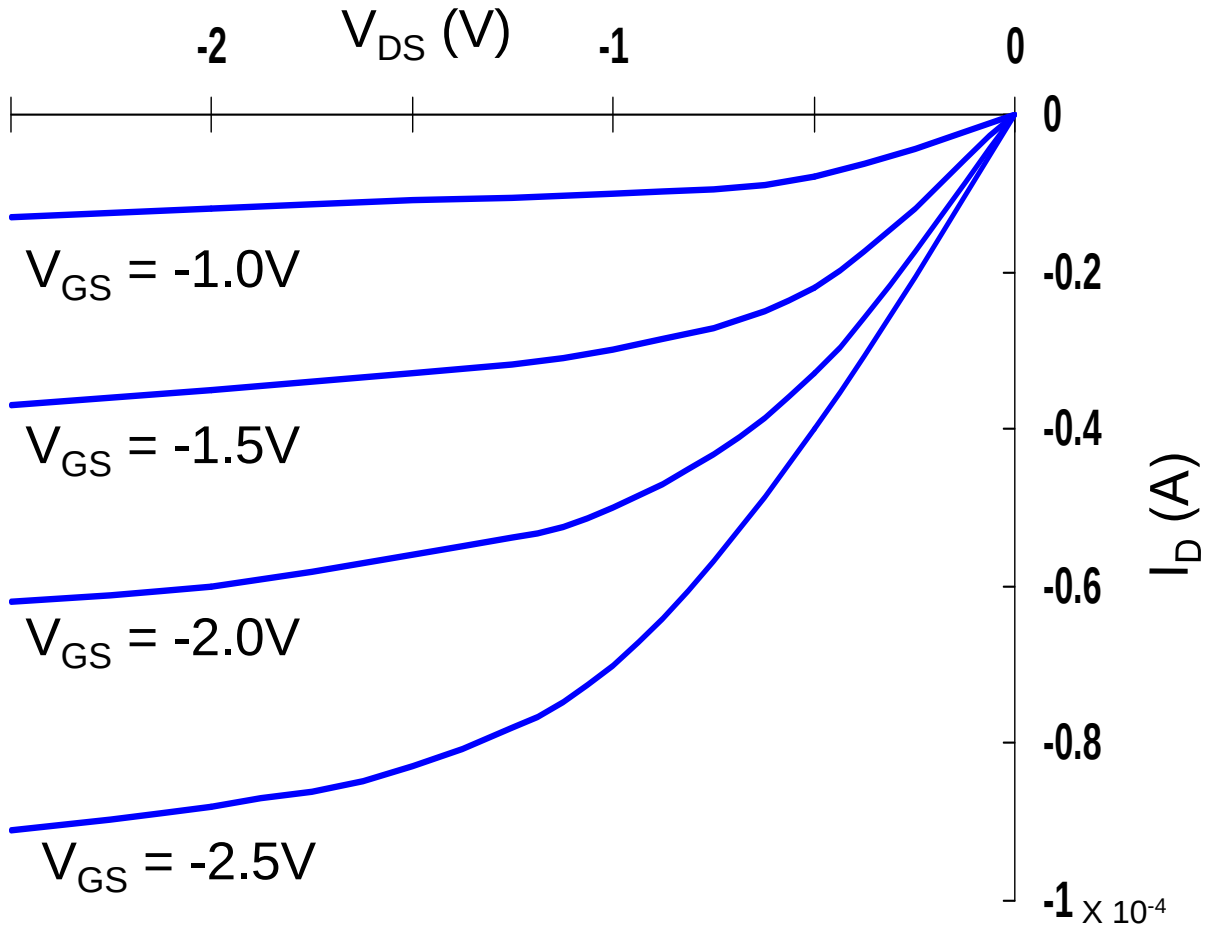
$\kappa(V) = 1/(1 + (V/\xi_c L))$ is a measure of the degree of velocity saturation

- Saturation: When $V_{DS} = V_{DSAT} \geq V_{GS} - V_T$

$$I_{DSat} = \kappa(V_{DSAT})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2]$$

Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



PMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = -0.4V

决定电流的主要因素

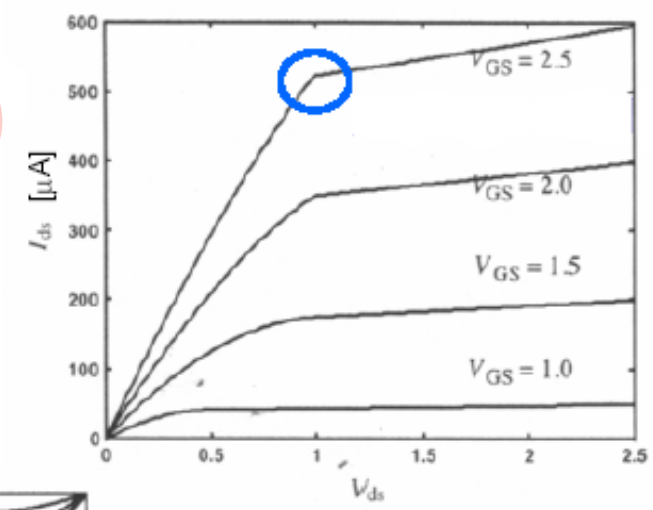
- 当 V_{DS} 和V_{GS} (> V_T), 固定时I_{DS} is 以下参数的函数
  - 沟道长： L
  - 沟道宽 – W
  - 阈值电压 – V_T
  - SiO2厚度 – t_{ox}
  - 栅极氧化膜的介电常数 (SiO_2) – ε_{ox}
  - 载流子迁移率
    - N型材料: μ_n = 500 cm^2/V-sec
    - P型材料: μ_p = 180 cm^2/V-sec

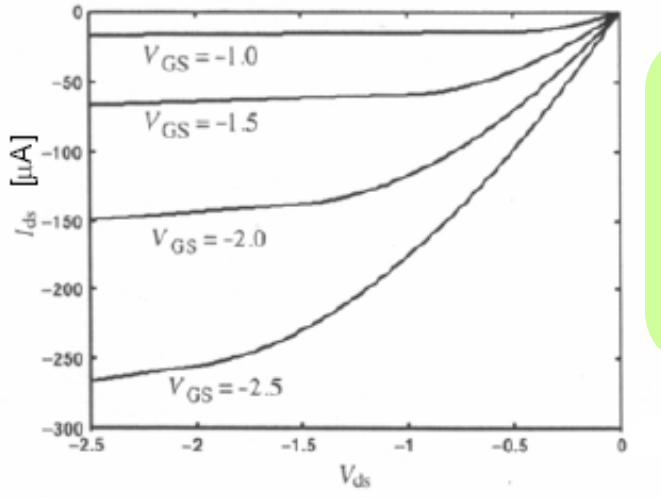
微小MOS晶体管的静态特性(沟道长小于1μm)

W/L=1.0μm/0.35μm

NMOS

- 当V_{DSAT}=1V，速度饱和





PMOS

- 迁移率是NMOS的一半
- 一般没有速度饱和

短沟道MOS晶体管电流解析式

$$I_{DS} = K_n' \cdot \frac{W}{L}\{(V_{GS} - V_{TH})V_{\min} - \frac{1}{2}V_{\min}\}(1 + \lambda V_{DS})$$

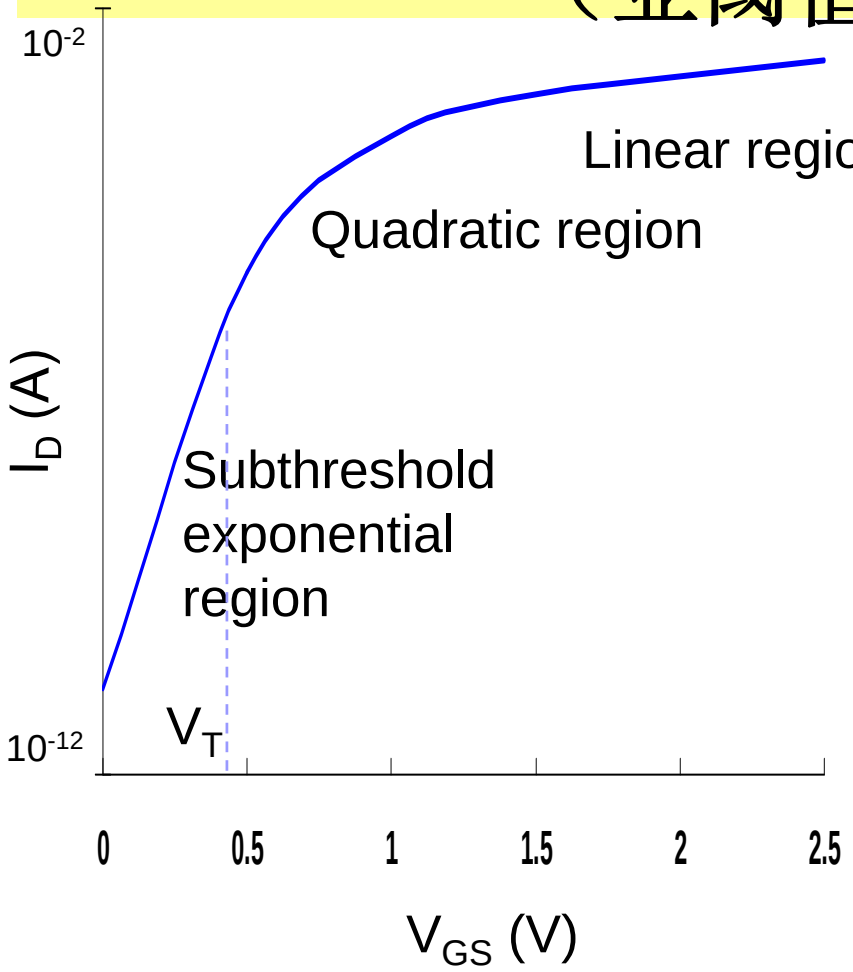
$$V_{\min} = (V_{GS} - V_{TH}, V_{DS}, V_{DSAT})$$

$$V_{TH} = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} - \gamma\sqrt{(2\phi_F - V_{BS})} + 2\phi_F$$

Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

Subthreshold Conductance
（亚阈值特性）



$I_D \sim I_S e^{(qV_{GS}/nkT)}$ where $n \geq 1$

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

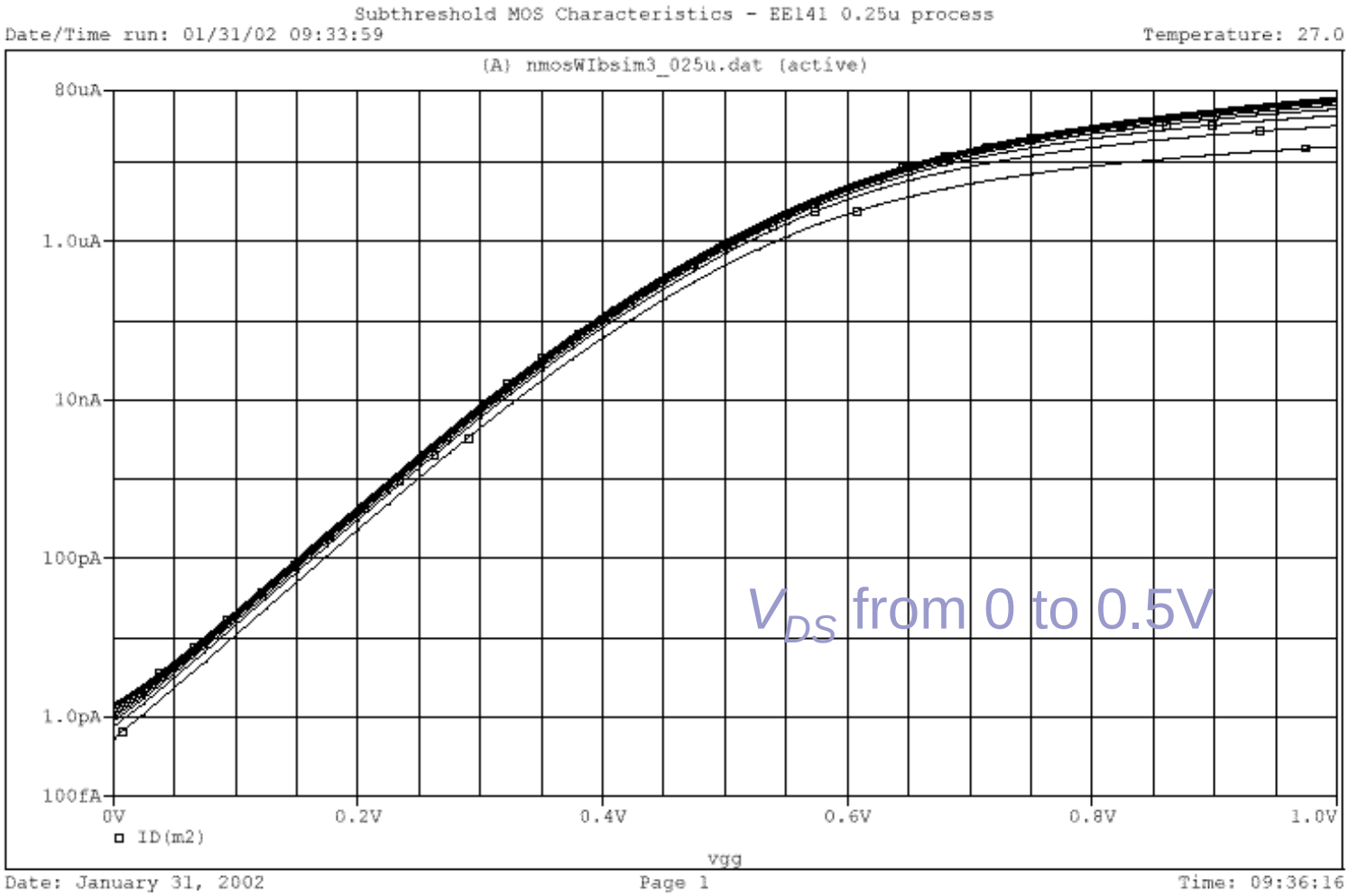
$$S = n\,(kT/q)\,\ln(10)$$

(typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

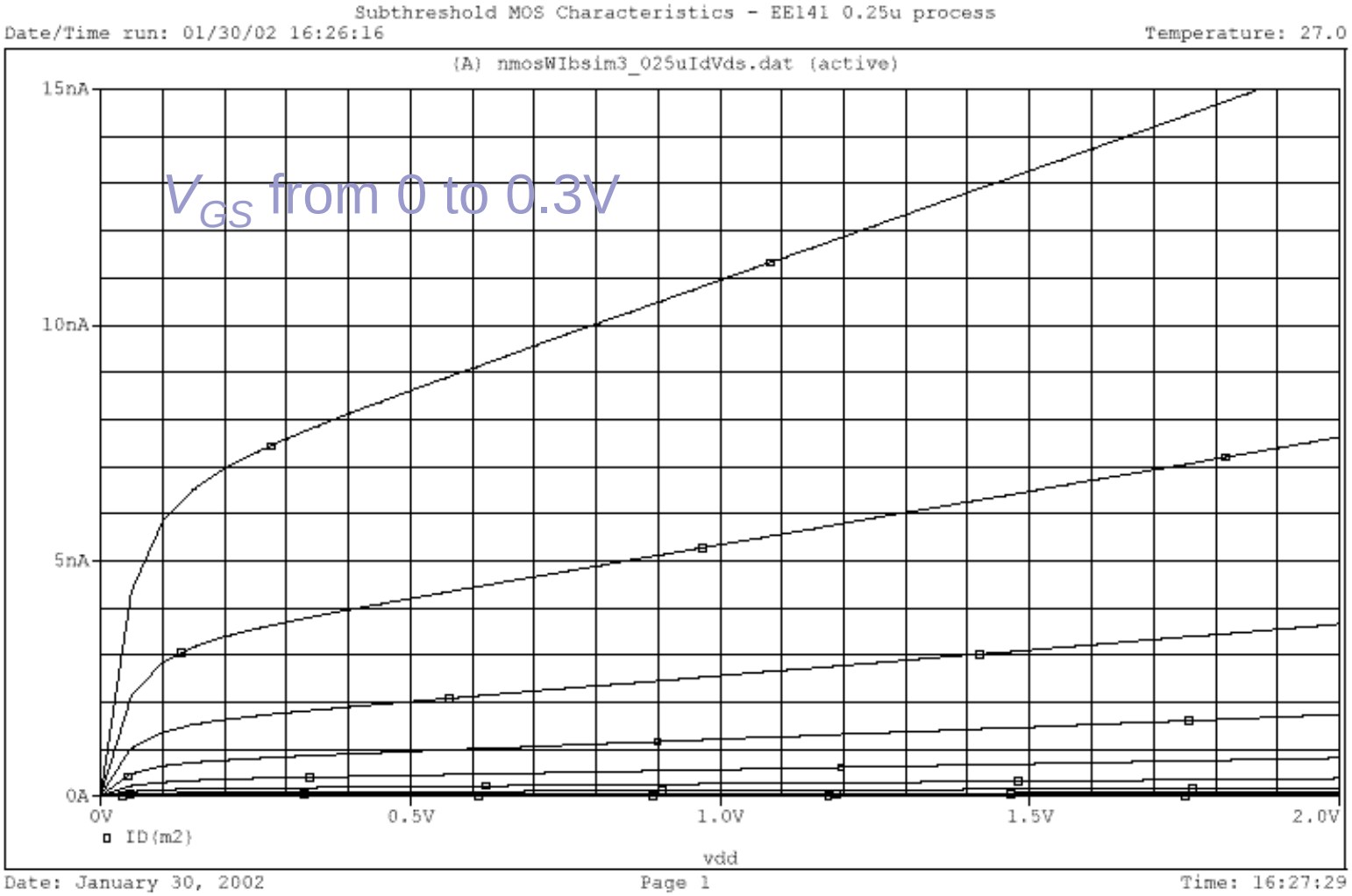
Subthreshold I_D vs V_{GS}

$$I_D = I_S\, e^{(qV_{GS}/nkT)}\ (1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$



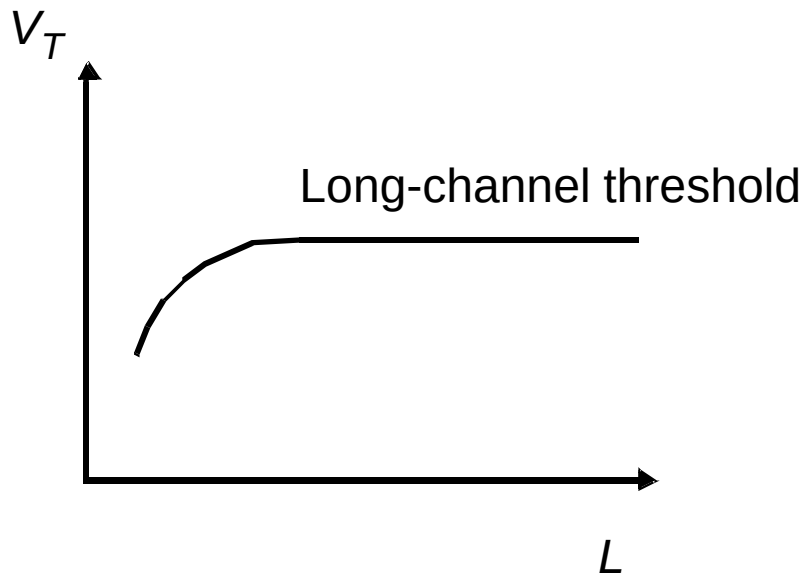
Subthreshold I_D vs V_{DS}

$$I_D = I_S\, e^{(qV_{GS}/nkT)}\ (1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$

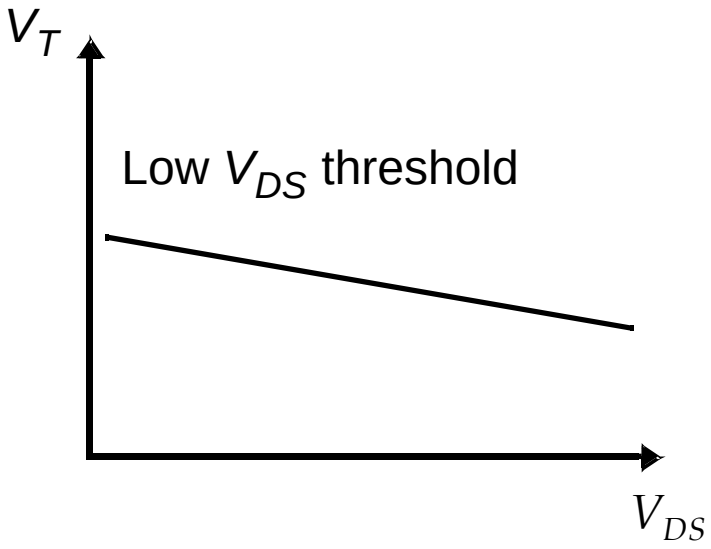


V_{GS} from 0 to 0.3V

Threshold Variations

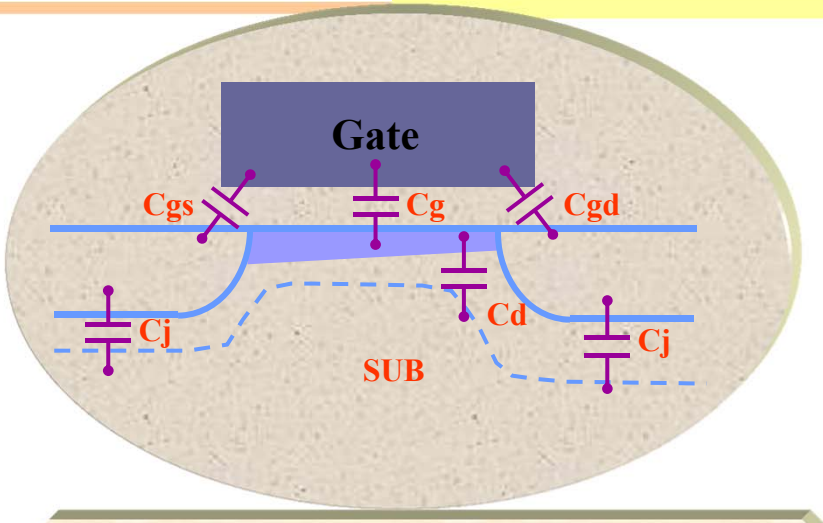


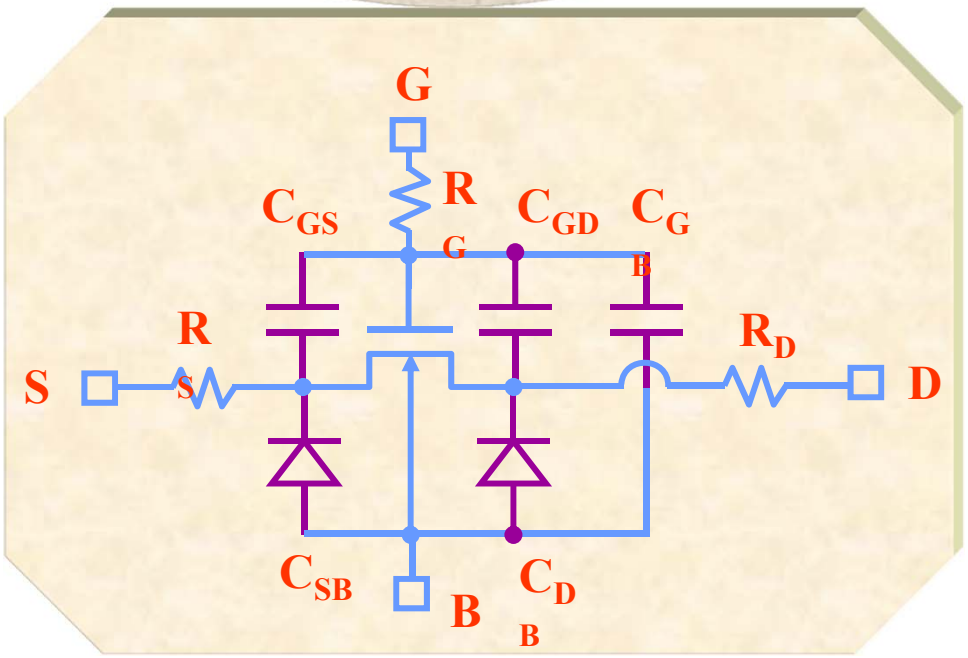
Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

MOSFET的电容





- MOSFET的电容决定其瞬态特性
- 寄生电阻与管子的导通电阻（数十KΩ）相比，通常可以忽略不计

例如：

栅极电容

C_{GS}, C_{GD}, C_{GB} (各为1.0fF)

漏源电容

C_{DB}, C_{SB} (各为0.5fF)

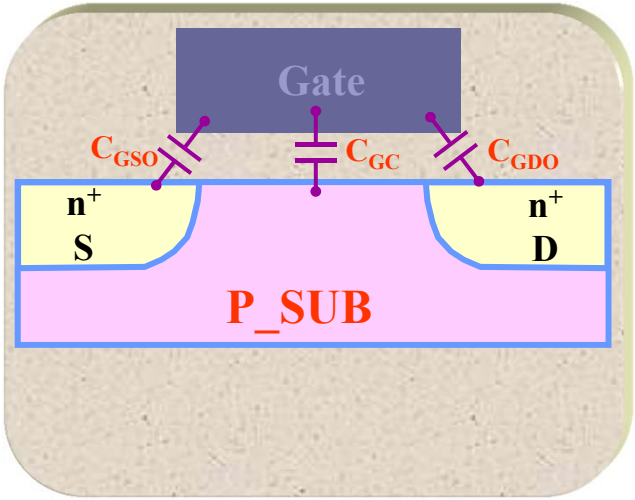
栅极电阻

R_G (40Ω)

源漏电阻

R_D, R_S (各1Ω)

MOSFET栅极电容

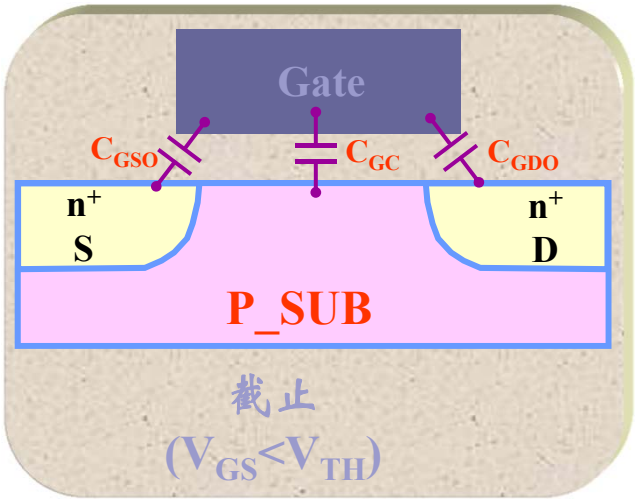


❖C_{GSO}和C_{GDO}—交叠电容，由源漏横向扩散形成，值一定

❖大多数情况下，忽略电压的影响，C_{GC}近似为CoxWL。根据MOSFET的工作区域，C_{GC}分配给C_{GD}，C_{GS}和C_{GB}。

$$c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

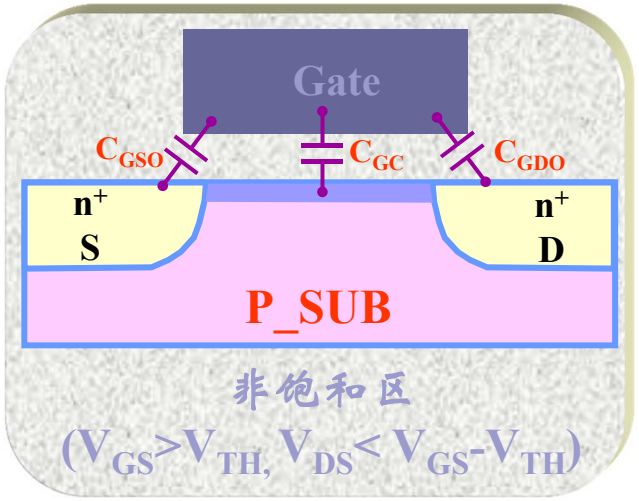
MOSFET栅极电容(cont.)



截止区：

沟道未形成，$C_{GD}=C_{GS}=0$, $C_{GB}=C_{GC}\approx C_{ox}WL$

MOSFET栅极电容(cont.)



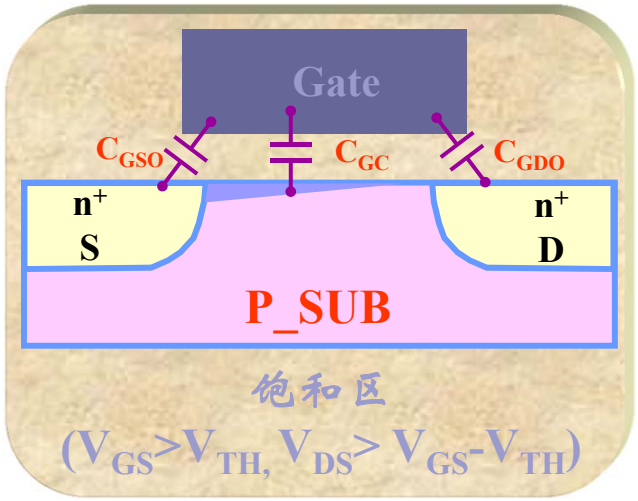
非饱和区：

沟道形成，相当于D、S连通，

$C_{GD}=C_{GS}\approx(1/2)\,CoxWL$

$C_{GB}=0$

MOSFET栅极电容(cont.)



饱和区：

漏端沟道夹断，$C_{GB}=0$，　$C_{GD}=0$

$$C_{GS}\approx(2/3)\,CoxWL$$

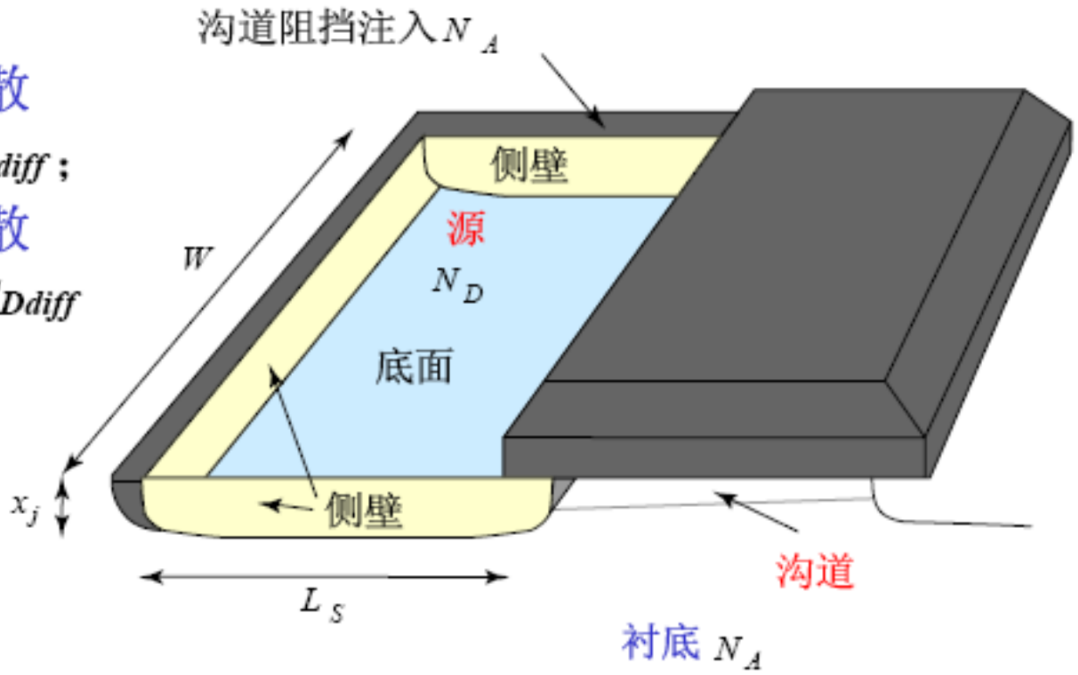
MOS晶体管的扩散(PN结)电容

源扩散

$C_{SB} = C_{sdiff}$;

漏扩散

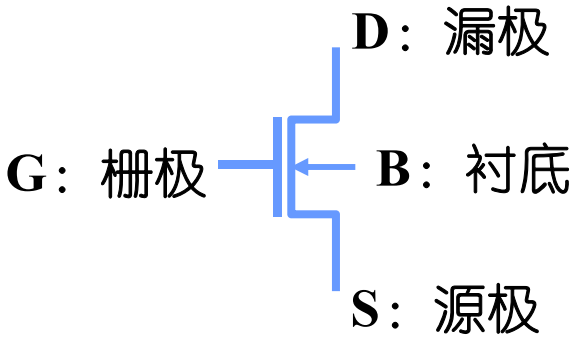
$C_{DB} = C_{Ddiff}$

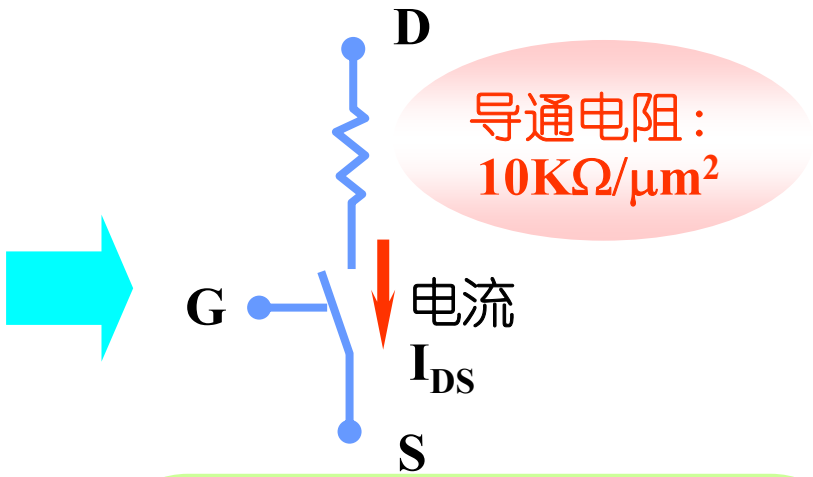


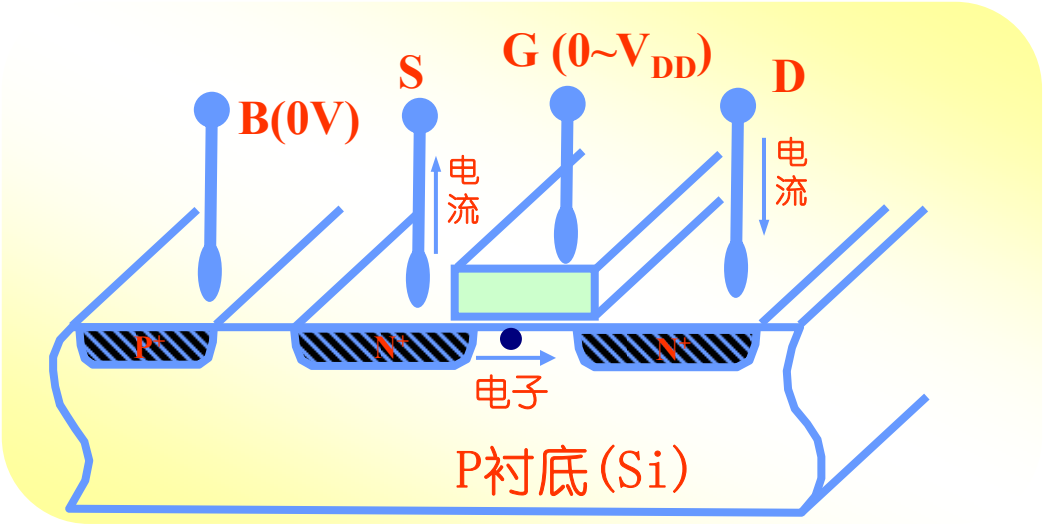
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

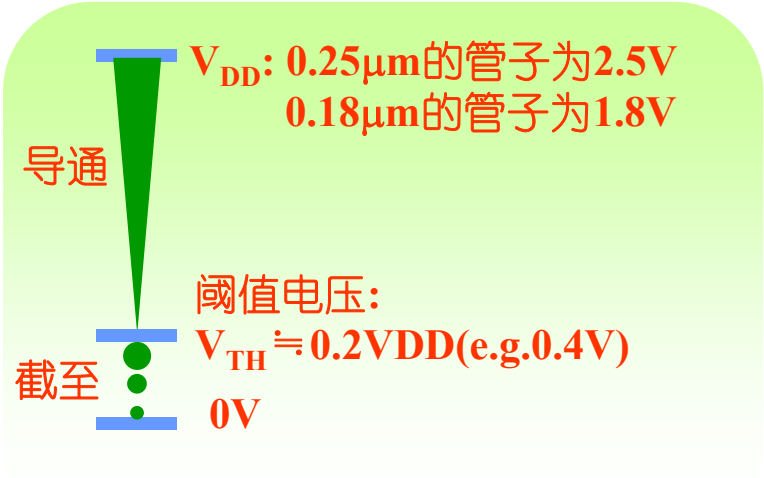
MOSFET的导通电阻

源极：载流子（电子）的供给源
漏极：载流子（电子）的排出口









MOS晶体管的导通电阻

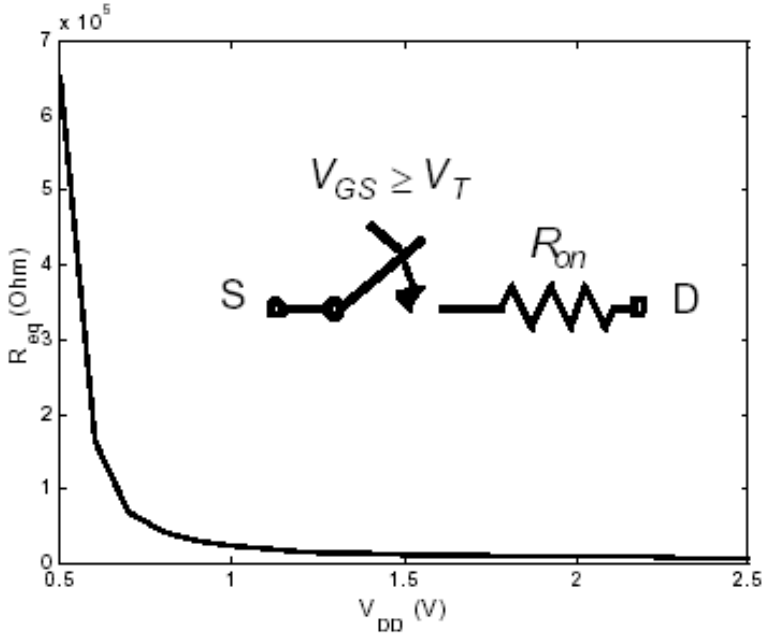
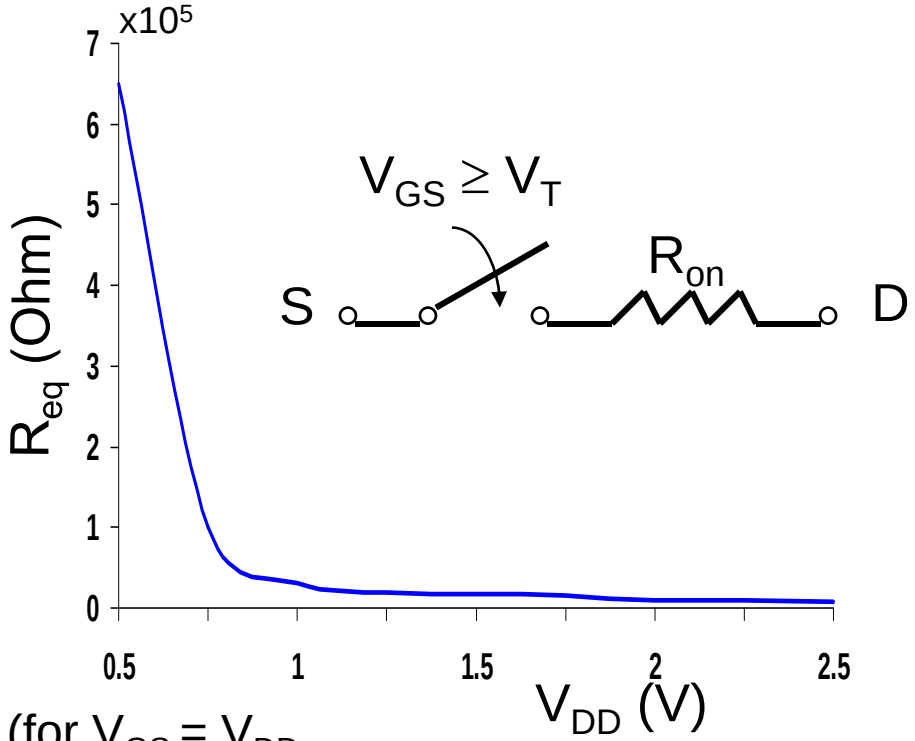


Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

The Transistor Modeled as a Switch



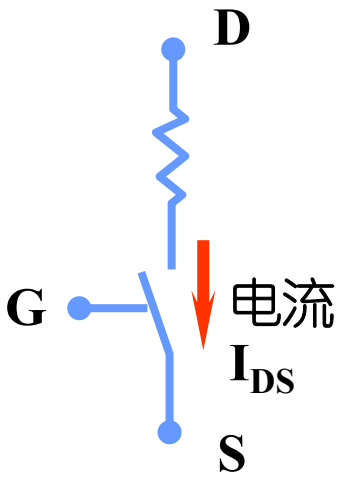
(for $V_{GS} = V_{DD}$, $V_{DS} = V_{DD} \rightarrow V_{DD}/2$)

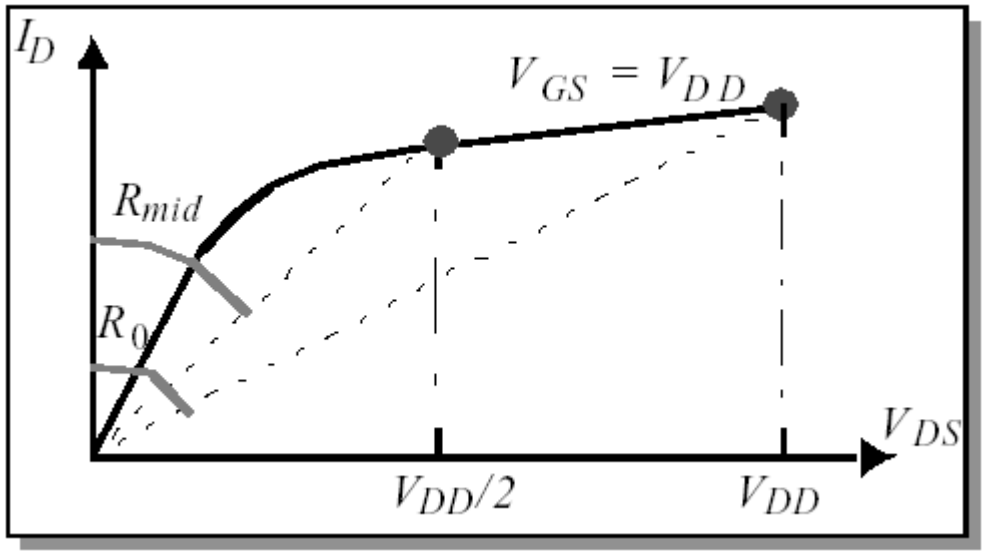
Modeled as a switch with infinite off resistance and a finite on resistance, R_{on}

- Resistance inversely proportional to W/L (doubling W halves R_{on})
- For $V_{DD} >> V_T + V_{DSAT}/2$, R_{on} independent of V_{DD}
- Once V_{DD} approaches V_T, R_{on} increases dramatically

V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

R_{on} (for W/L = 1)
For larger devices divide R_{eq} by W/L





- 导通电阻是一个非线性电阻，与器件的工作状态有关,平均电阻一般取**0.75R_0**
- 在非饱和区，导通电阻近似为线性电阻

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$ 即**R_{on}=1/g_m**

- 导通电阻反比于（**W/L)**，**W**每增加一倍，电阻减小一半