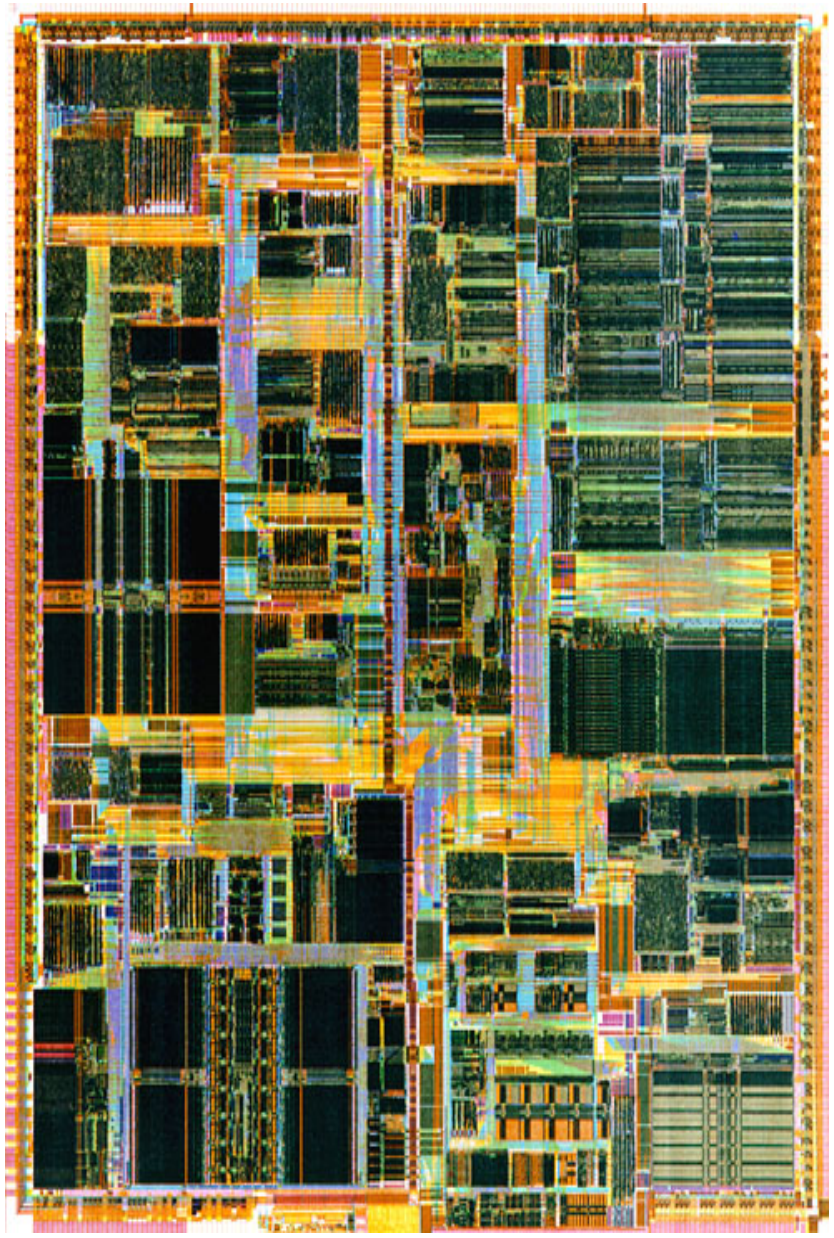
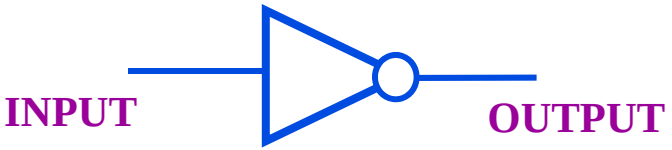


半导体集成电路

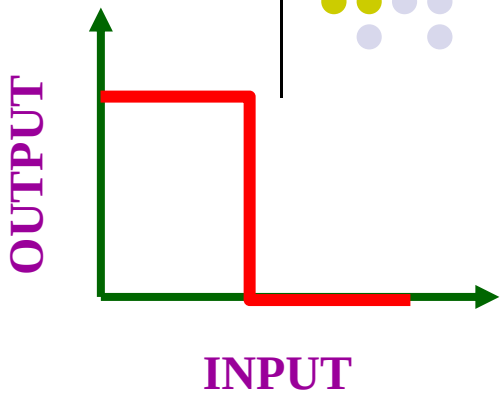
学校：西安理工大学
院系：自动化学院电子工程系
专业：电子、微电
时间：秋季学期

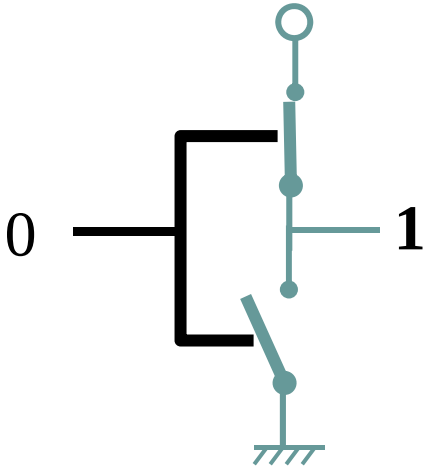
上一章内容要点

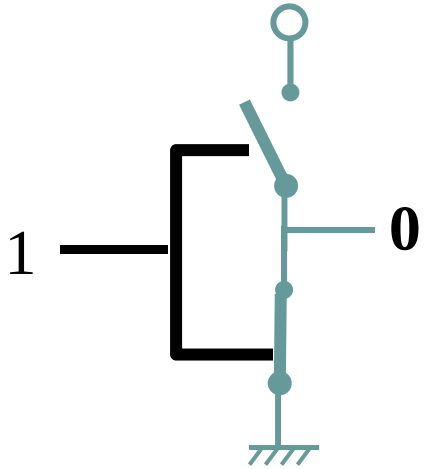
CMOS反相器基本概念

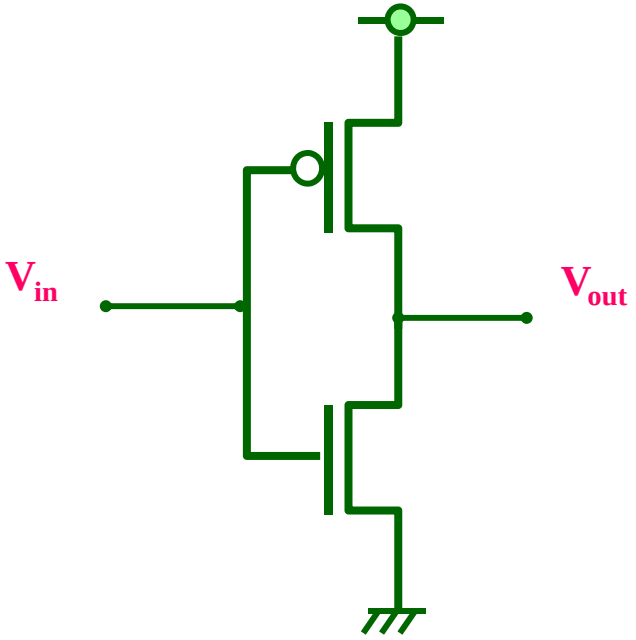


INPUT	OUTPUT
0	1
1	0

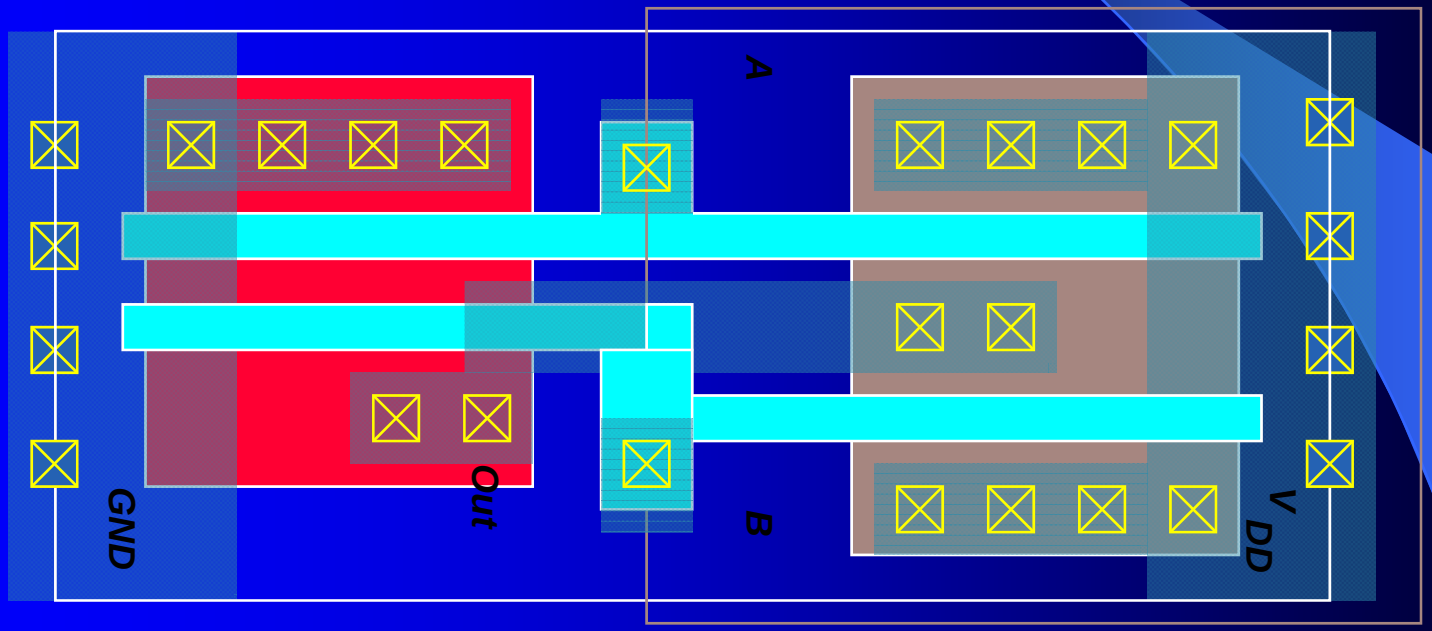








第6章 CMOS静态逻辑门电路

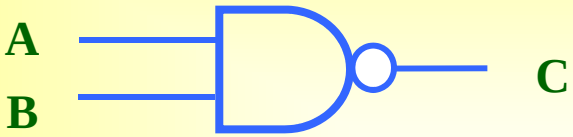


内容提要

- CMOS静态逻辑门：CMOS与非门或非门、复合门的构成
- CMOS门电路的速度（延迟）
- CMOS门电路的功耗

6.1 CMOS静态组合逻辑单元

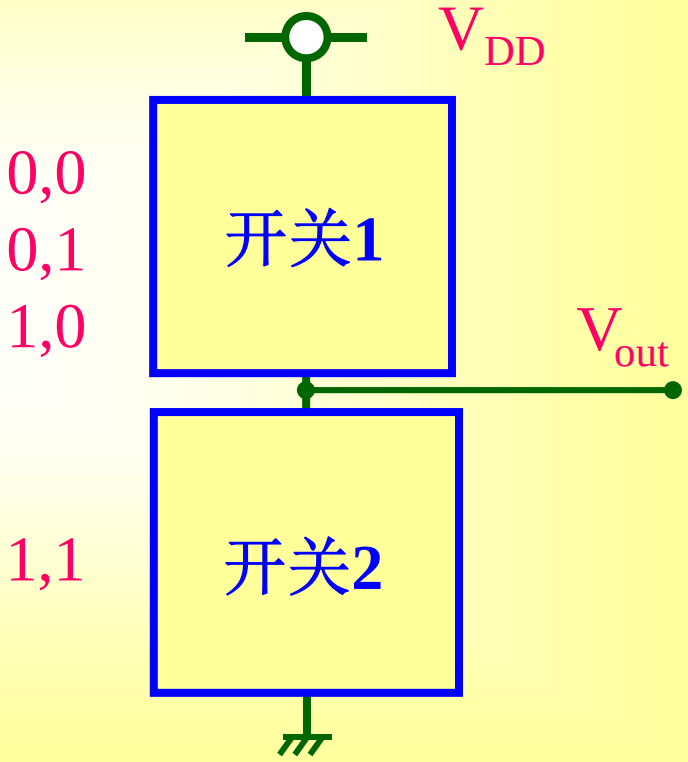
1.CMOS与非门



$C=\overline{A \cdot B}$

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

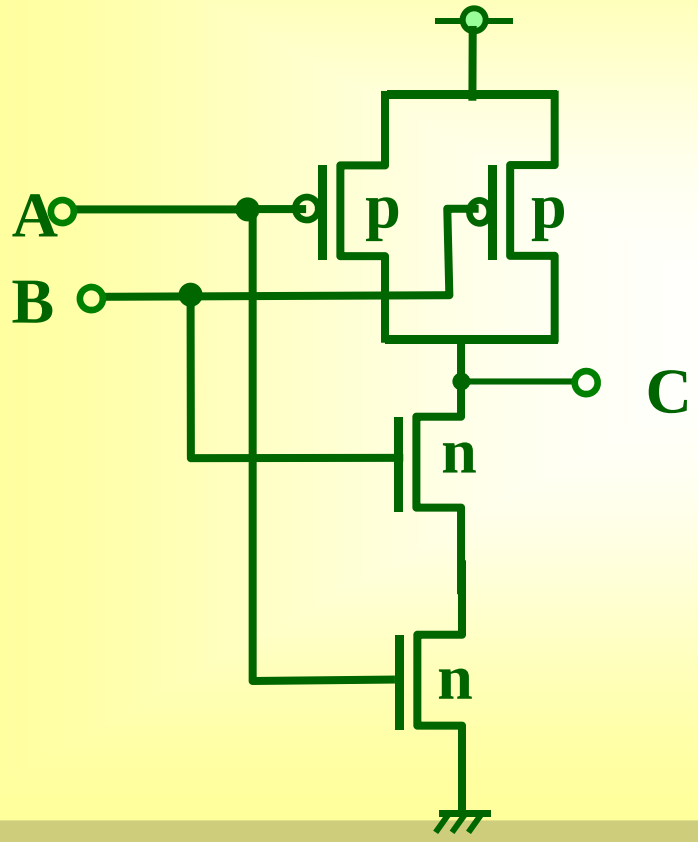
电路如何实现？

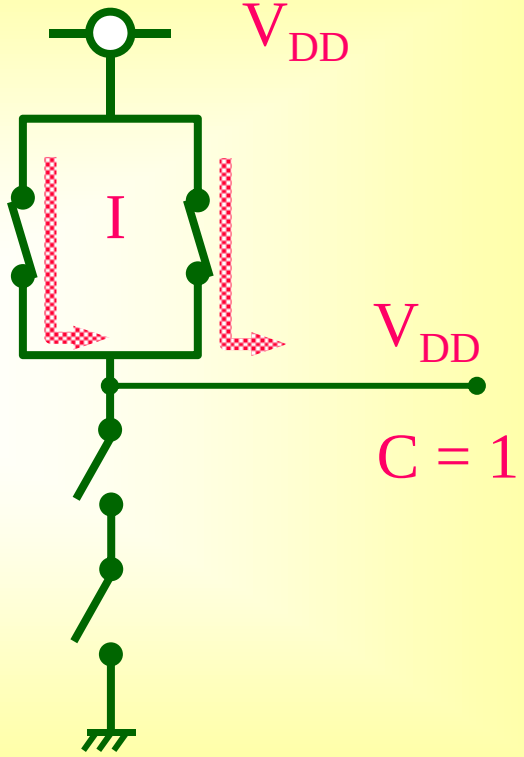


CMOS与非门动作原理-1

A = 0
B = 0

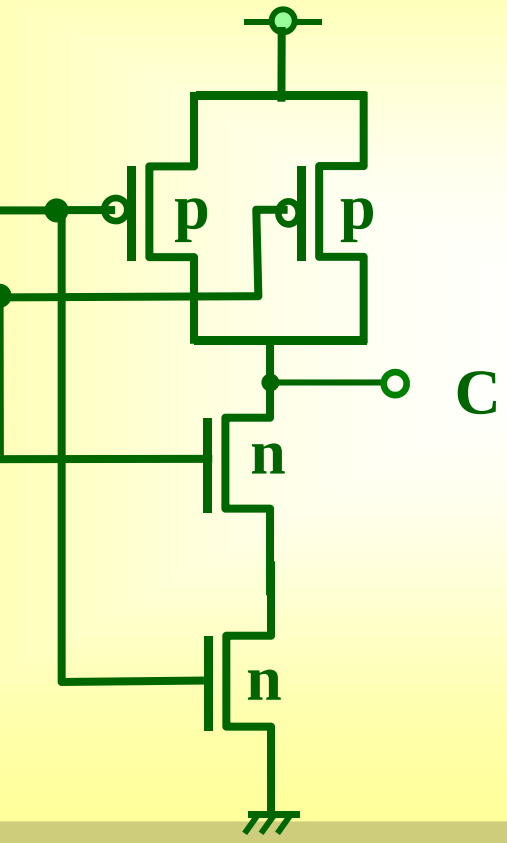
C = 1

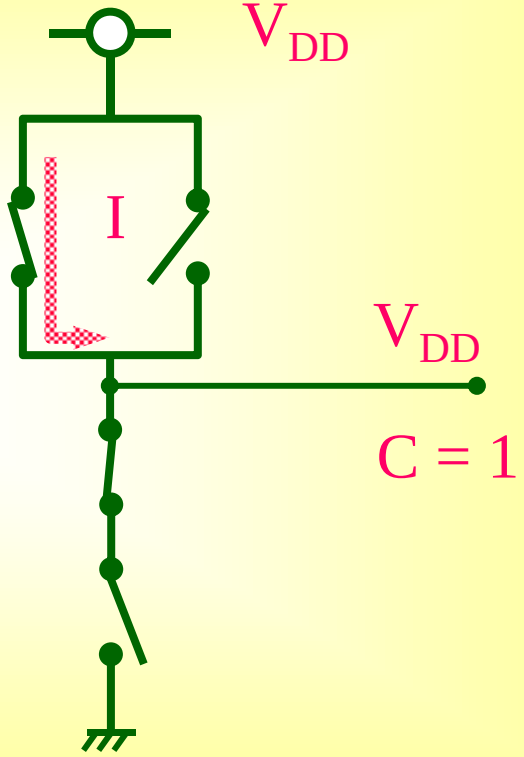




CMOS与非门动作原理-2

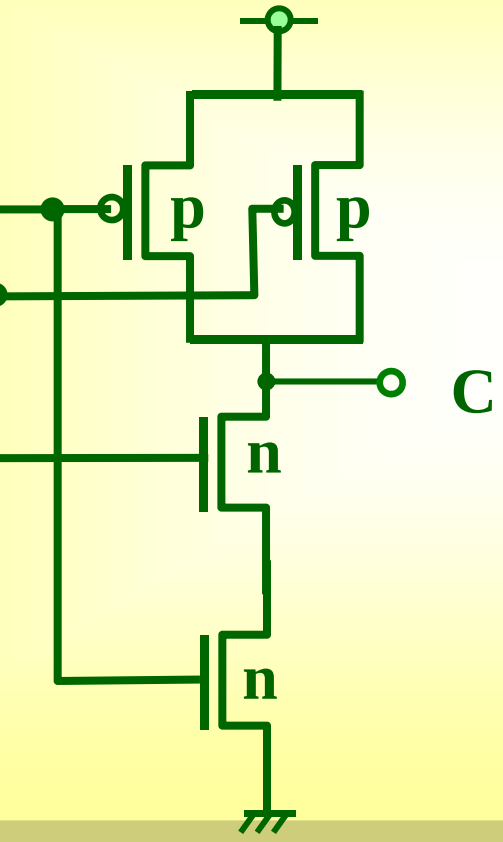
A = 0
B = 1

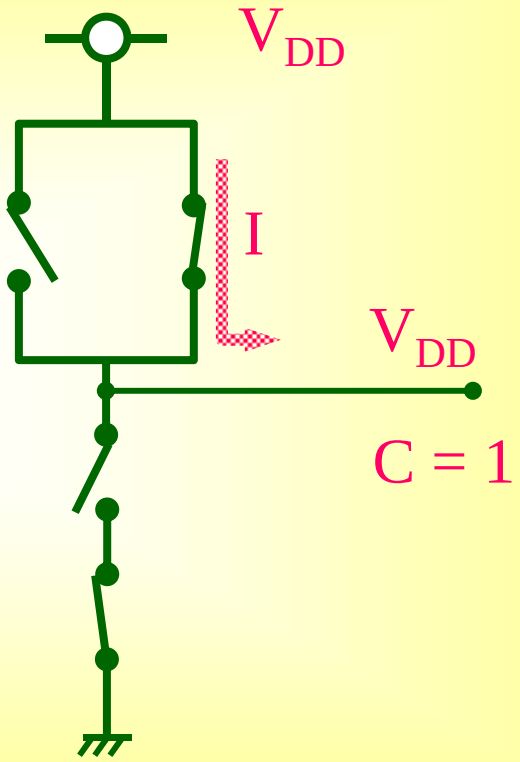




CMOS与非门动作原理-3

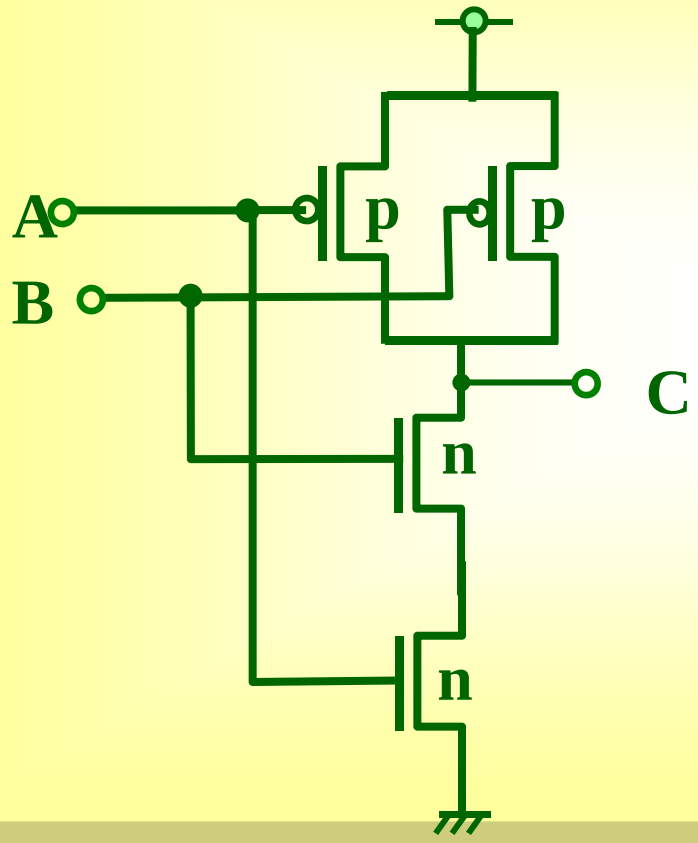
A = 1
B = 0



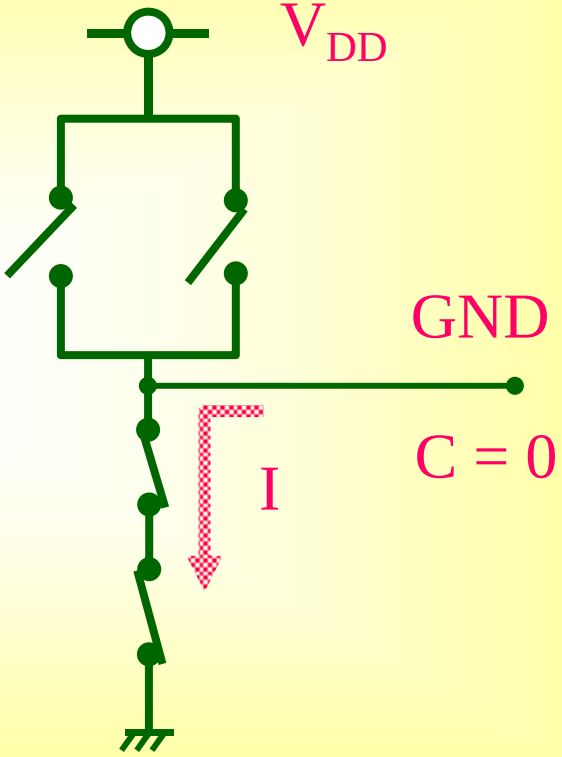


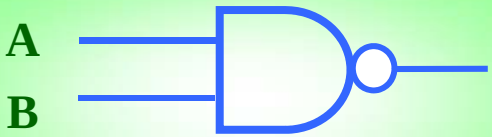
CMOS与非门动作原理-4

A = 1
B = 1



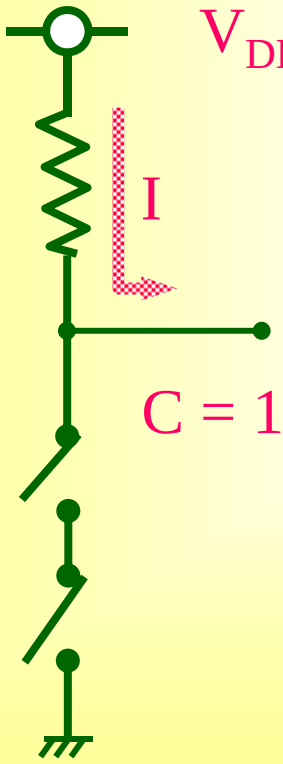
C = 0



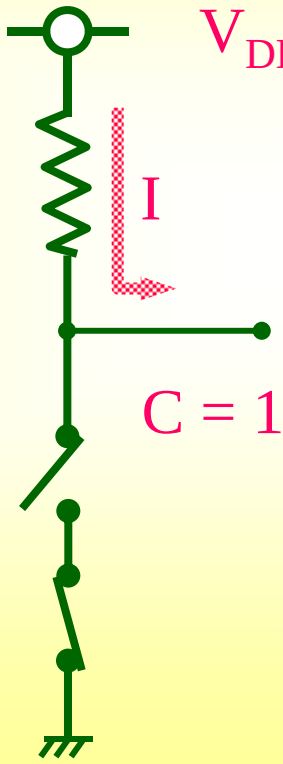


$C=\overline{A \cdot B}$

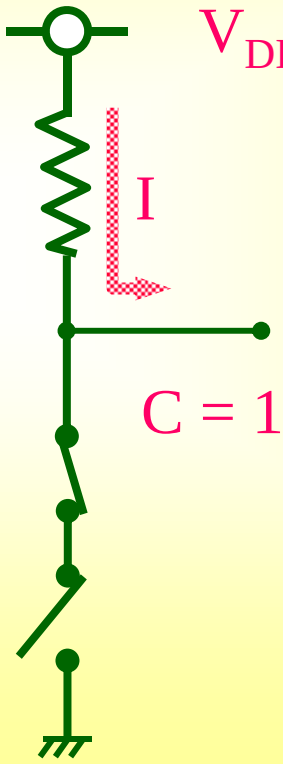
A = 0
B = 0



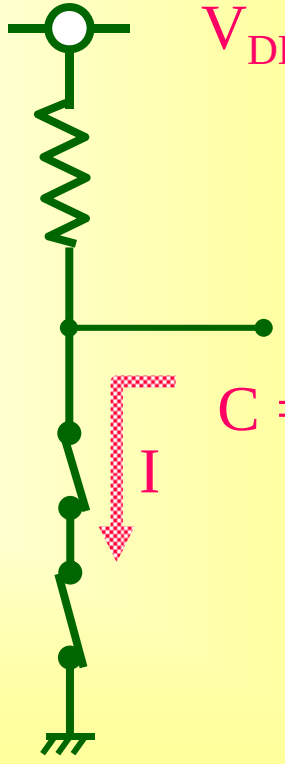
A = 0
B = 1



A = 1
B = 0

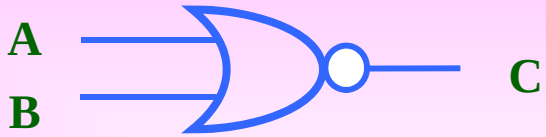


A = 1
B = 1



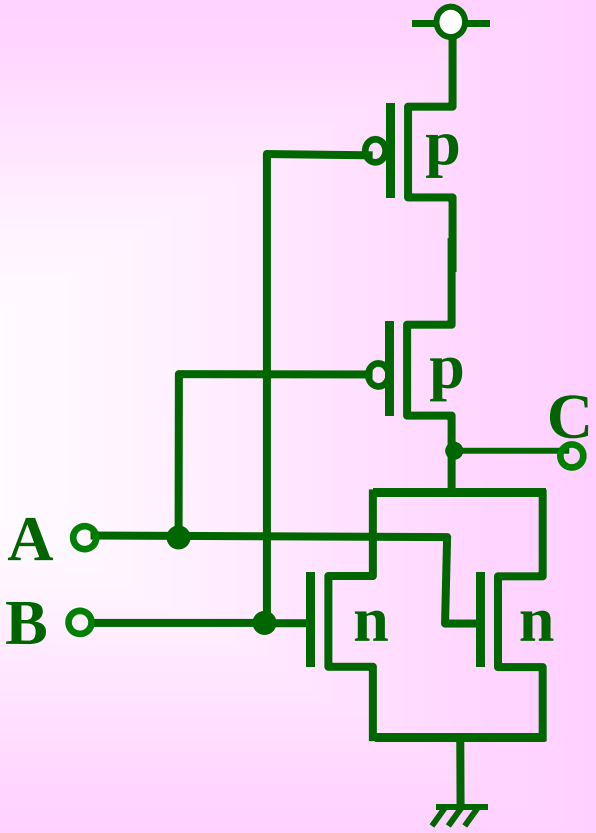
CMOS静态组合逻辑门

2.CMOS或非门



$C=\overline{A+B}$

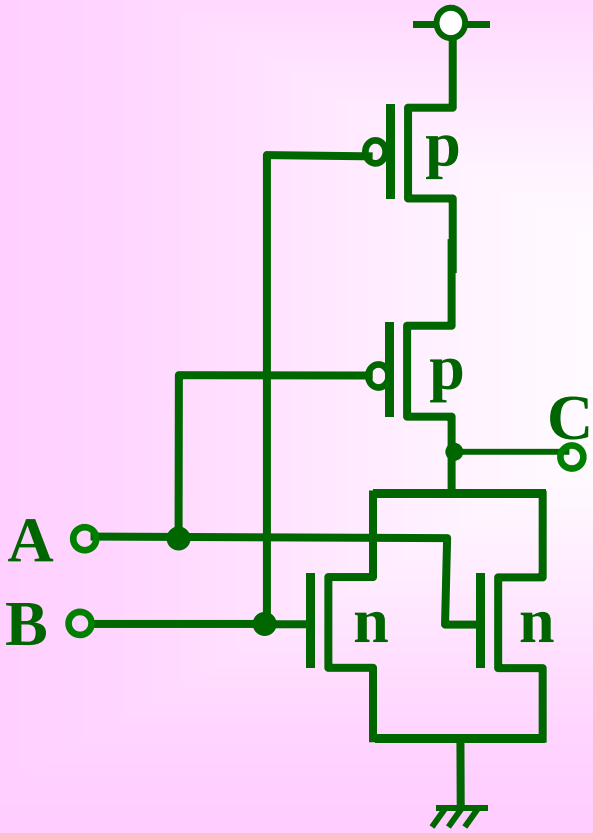
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

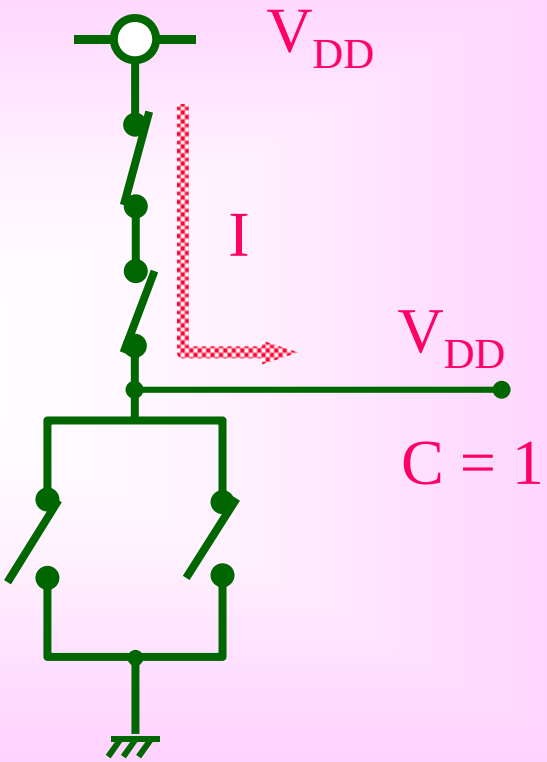


或非门动作原理-1

A = 0
B = 0

C = 1

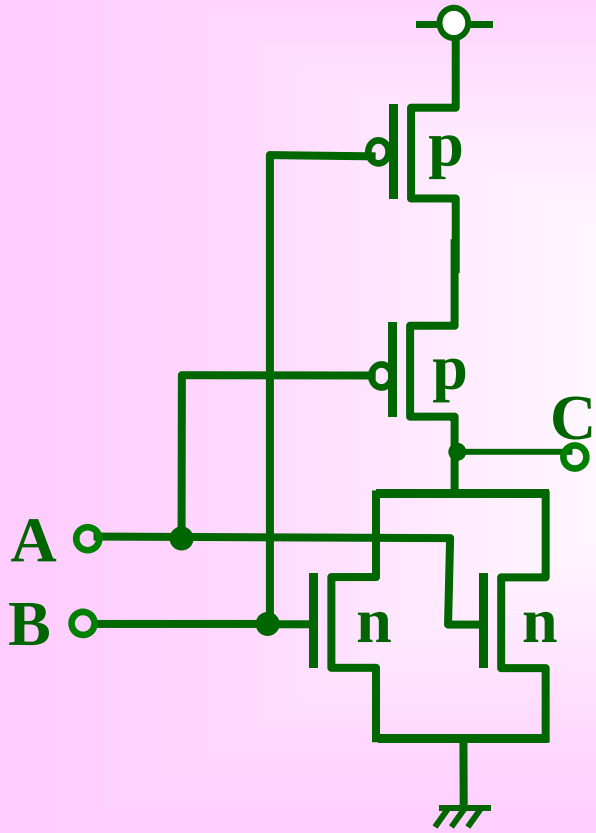


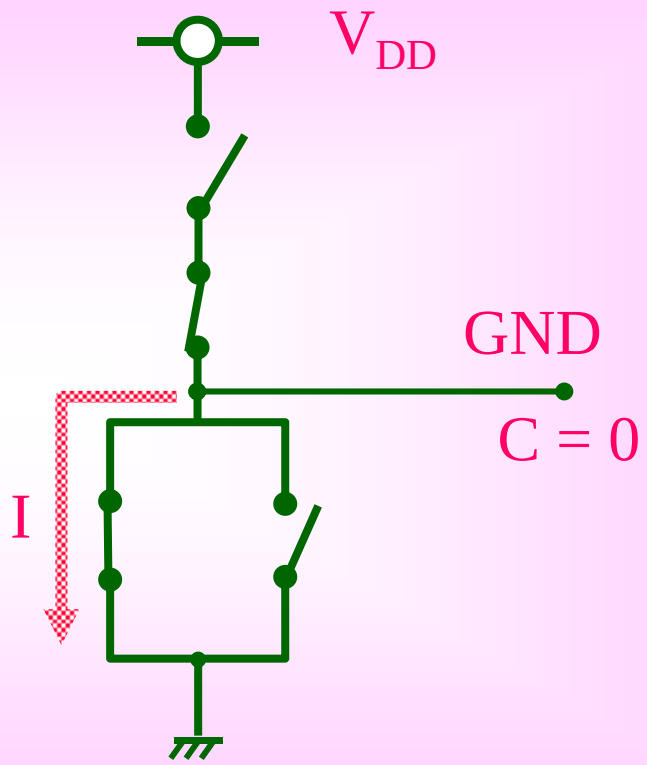


或非门动作原理-2

A = 0
B = 1

C = 0

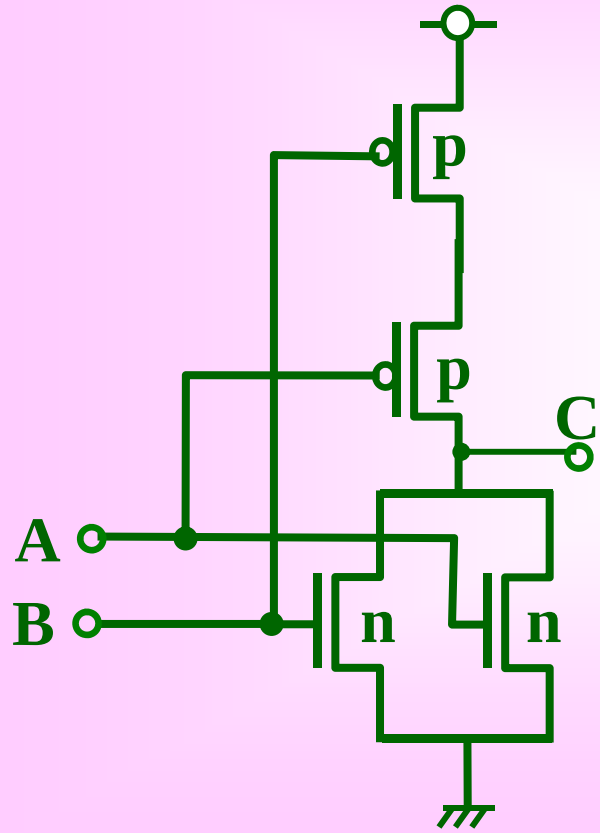


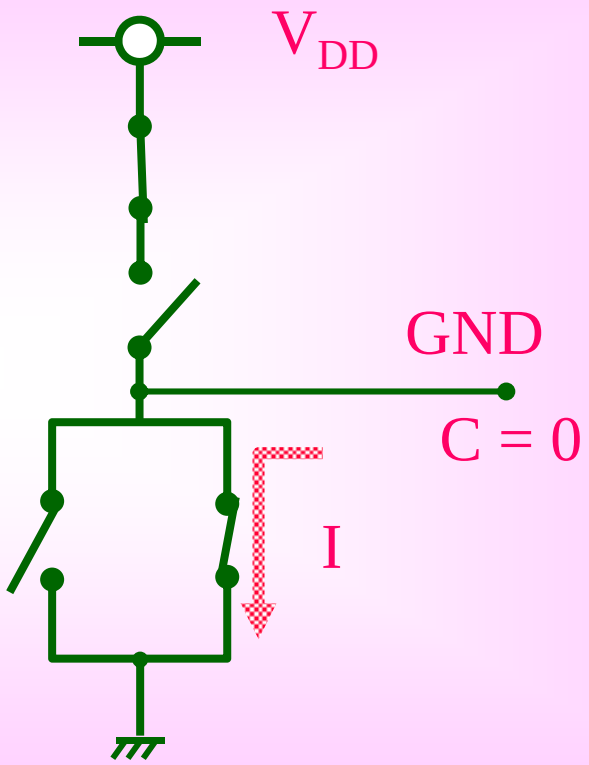


或非门动作原理-3

A = 1
B = 0

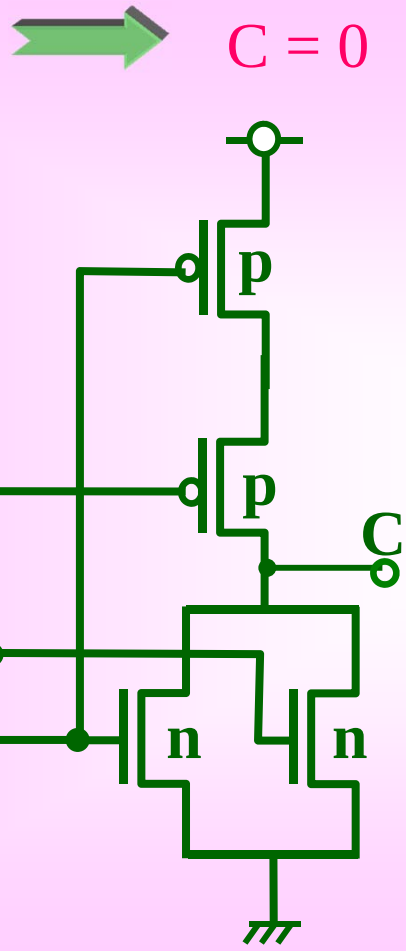
C = 0



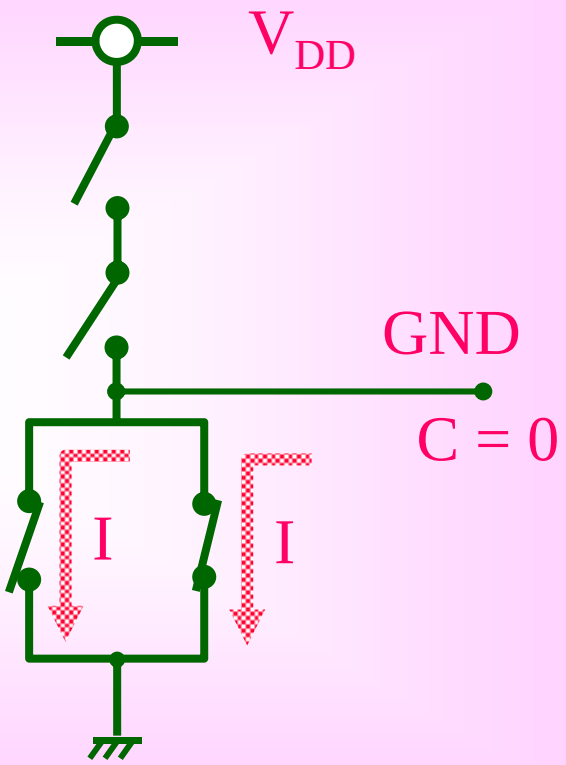


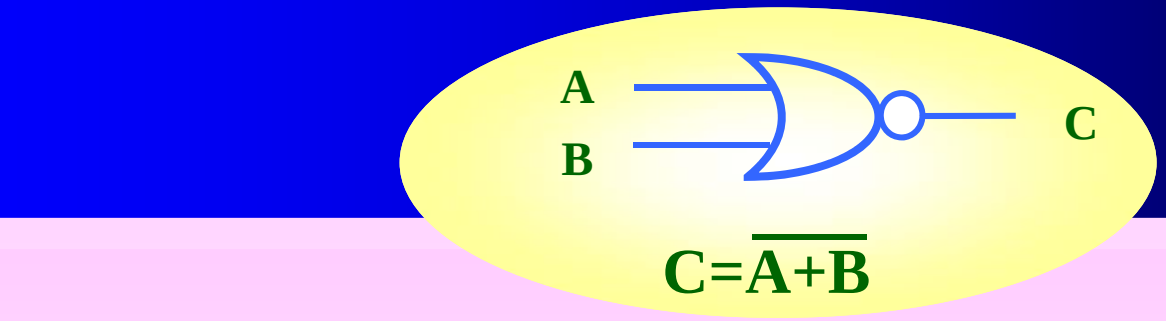
或非门动作原理-4

A = 1
B = 1

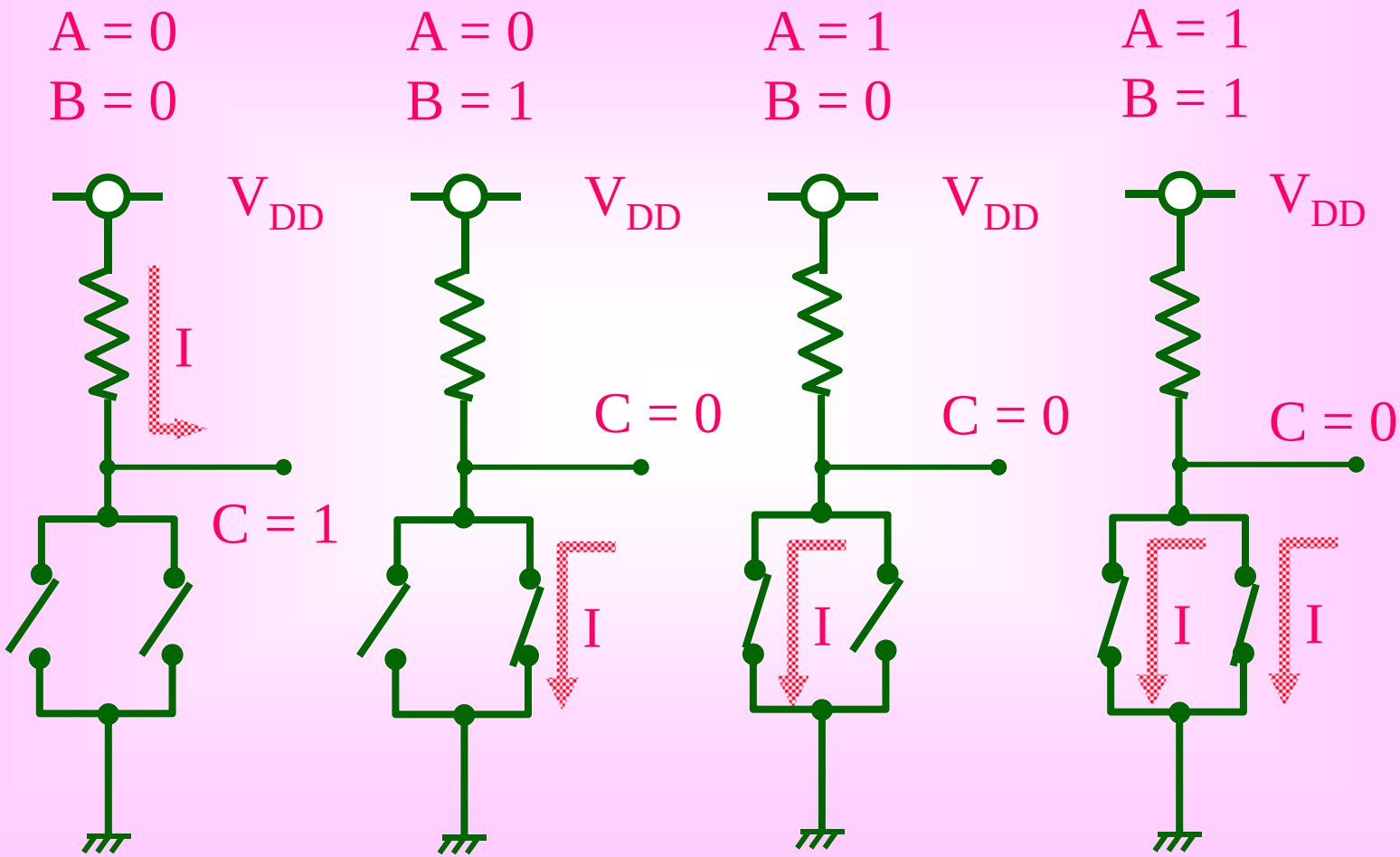


C = 0



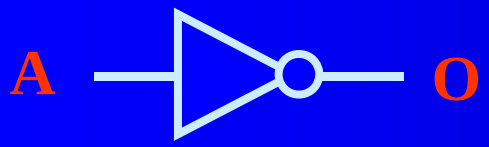


$C=\overline{A+B}$

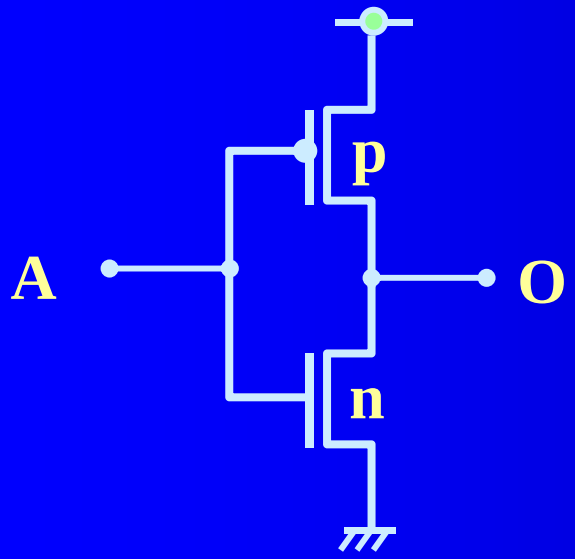


基本CMOS逻辑门--1

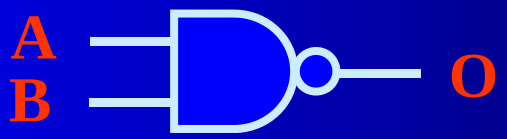
反相器



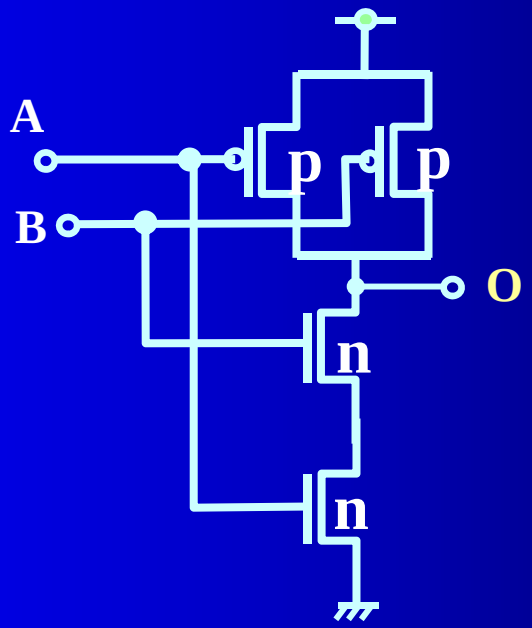
$O=\overline{A}$



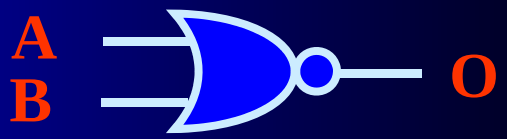
两输入与非门



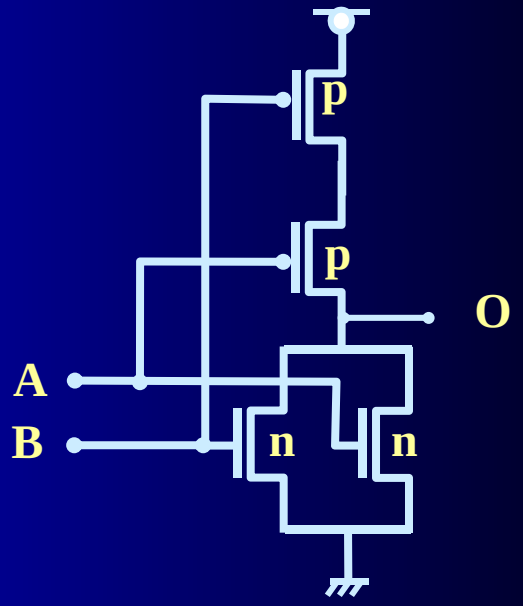
$O=\overline{A \cdot B}$



两输入或非门



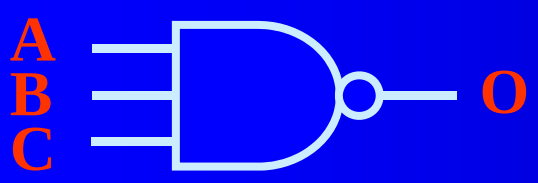
$O=\overline{A+B}$



逻辑门的设计

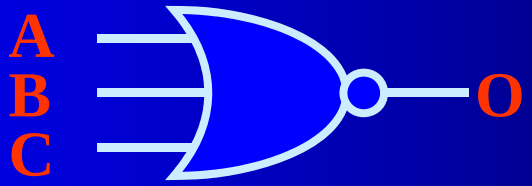
基本CMOS逻辑门--2

三输入与非门

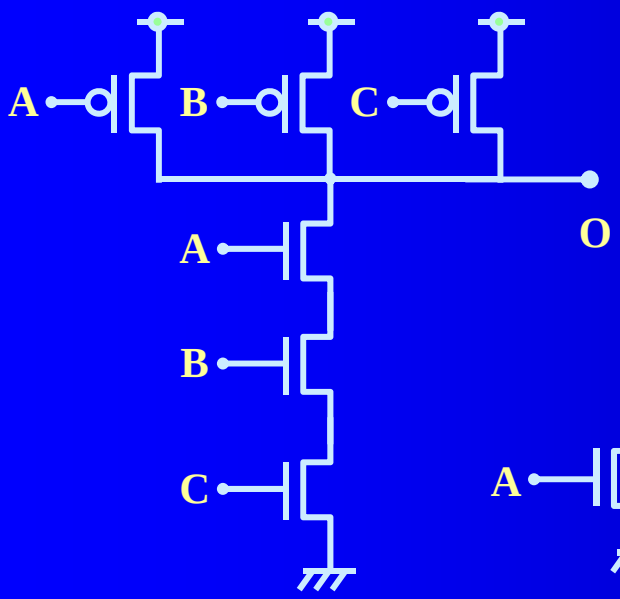


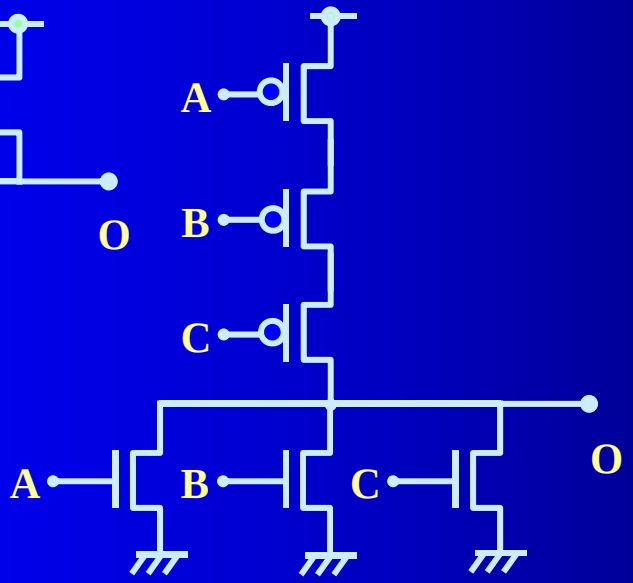
$O=\overline{A\cdot B\cdot C}$

三输入或非门



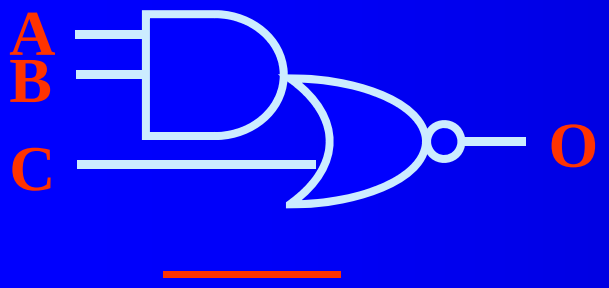
$O=\overline{A+B+C}$



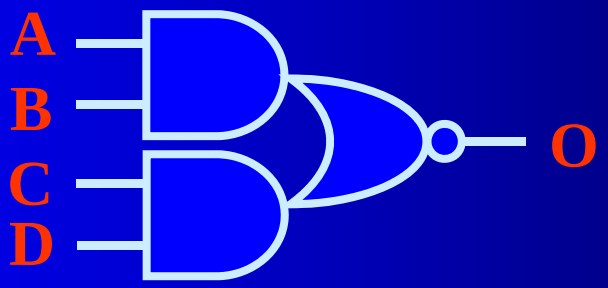


- NMOS、PMOS互补：
  （并联《====》串联）
  NMOS→ 输出为“0”
  PMOS→ 输出为“1”
- 生成电路为负逻辑：
  组成AND和OR时，
  加一反相器。
- 晶体管数为：
  输入端 子数的两倍。

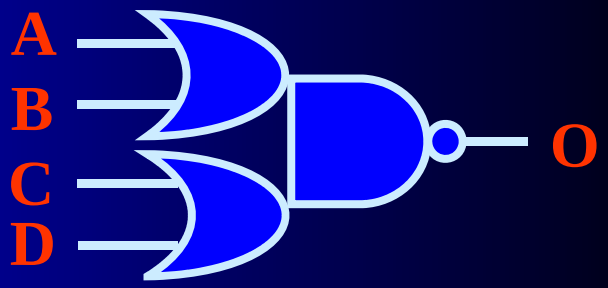
复合逻辑门



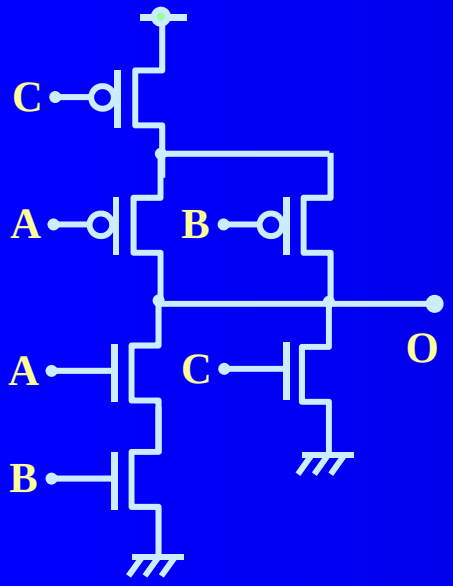
$O=\overline{A\cdot B+C}$

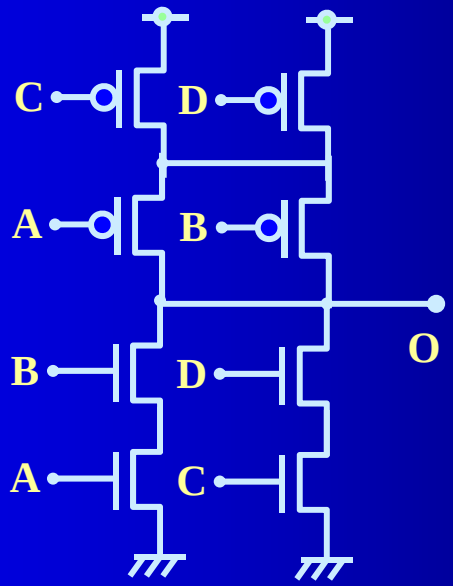


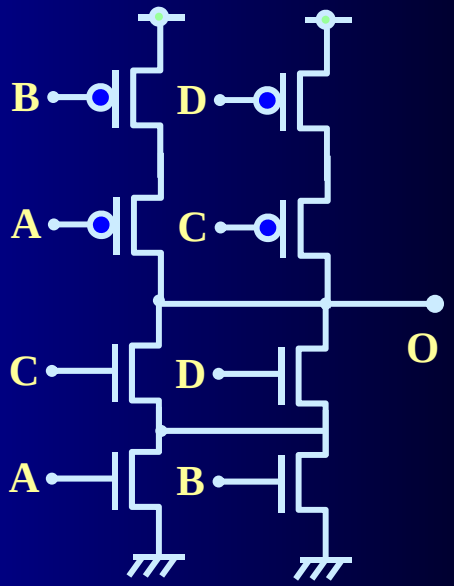
$O=\overline{A\cdot B+C\cdot D}$



$O=\overline{(A+B)\cdot(C+D)}$



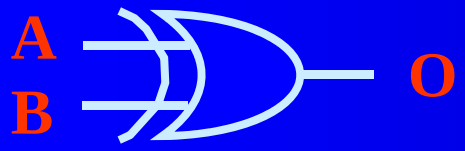




逻辑门的设计

Exclusive OR 逻辑门

2输入EOR（异或门）



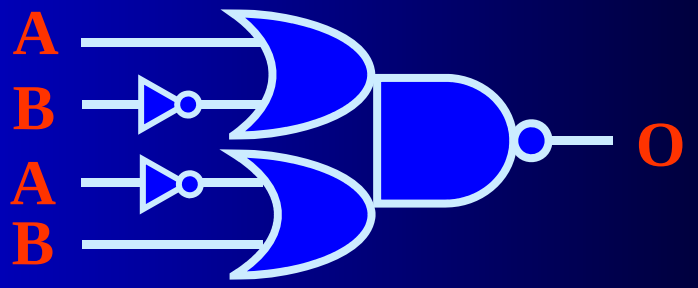
A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

$$O = \overline{A}\cdot B + A\cdot\overline{B}$$

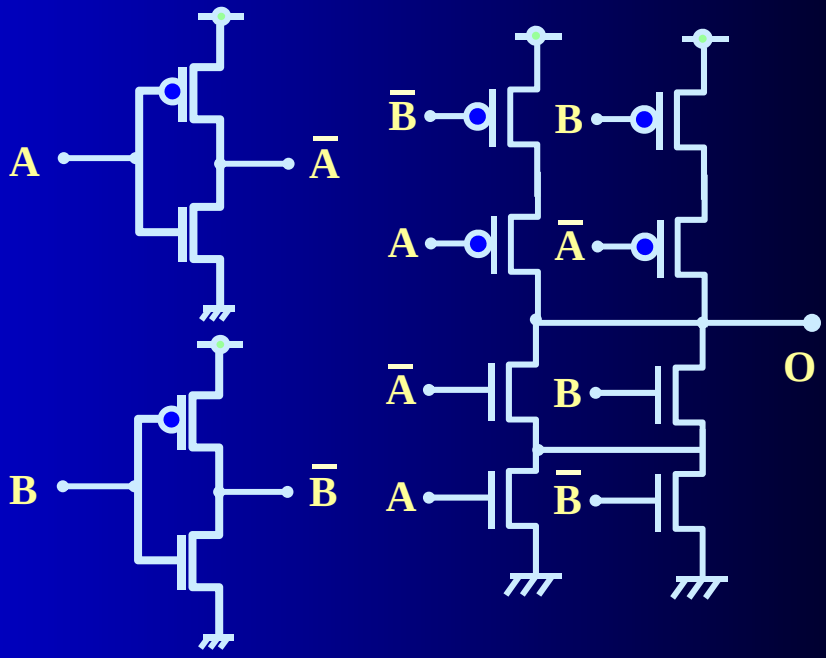
$$= \overline{\overline{A}\cdot B + A\cdot\overline{B}}$$

$$= \overline{(\overline{A}\cdot B)\cdot(A\cdot\overline{B})}$$

$$= \overline{(A+\overline{B})\cdot(\overline{A}+B)}$$



$$O = \overline{(A+\overline{B})\cdot(\overline{A}+B)}$$

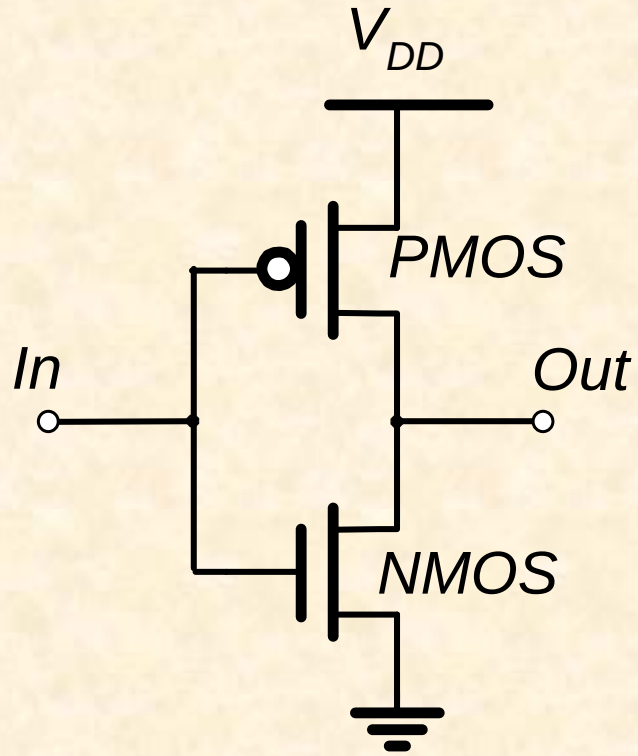


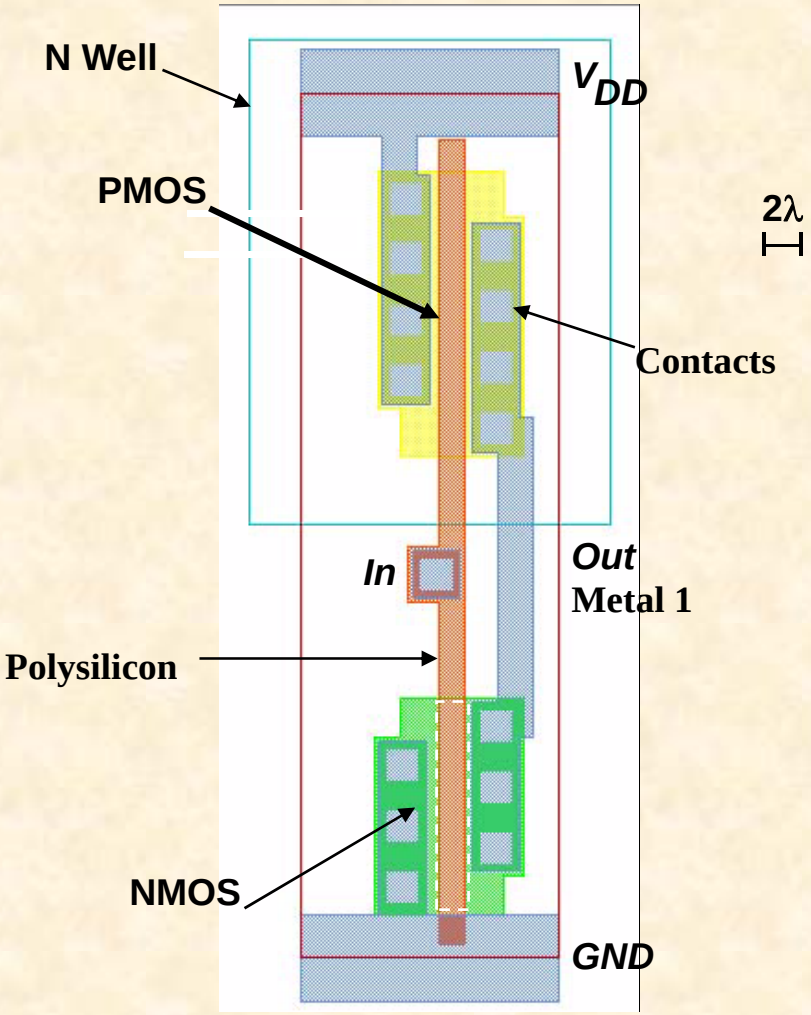
复合逻辑门

- 调整逻辑关系式，使得输出为负逻辑
- 逻辑关系为与时，**NMOS**串联、**PMOS**并联
- 逻辑关系为或时，**NMOS**并联、**PMOS**串联
- 改变尺寸可调整输入阈值或速度

IC版图对应于线路

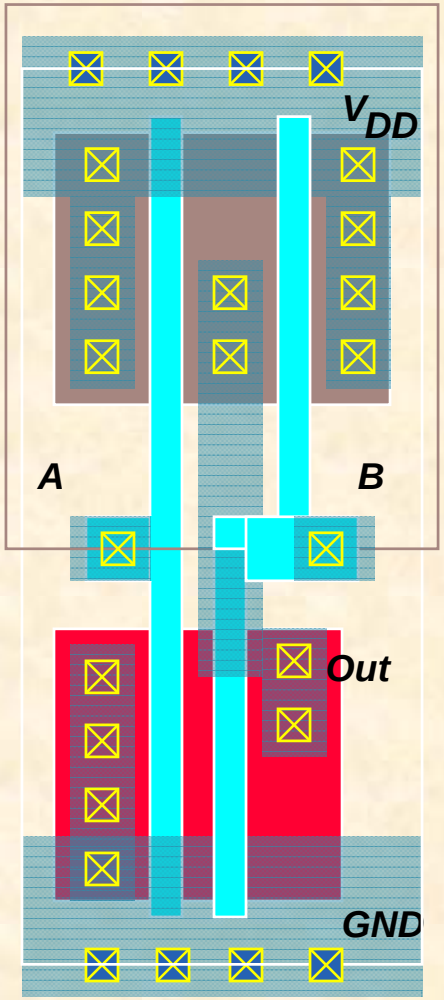
反相器

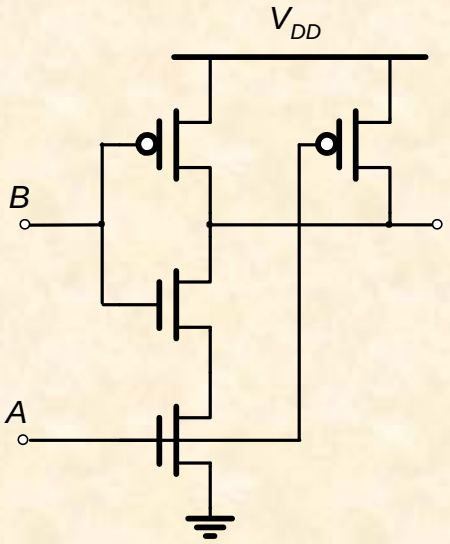




IC版图对应于线路

2-NAND

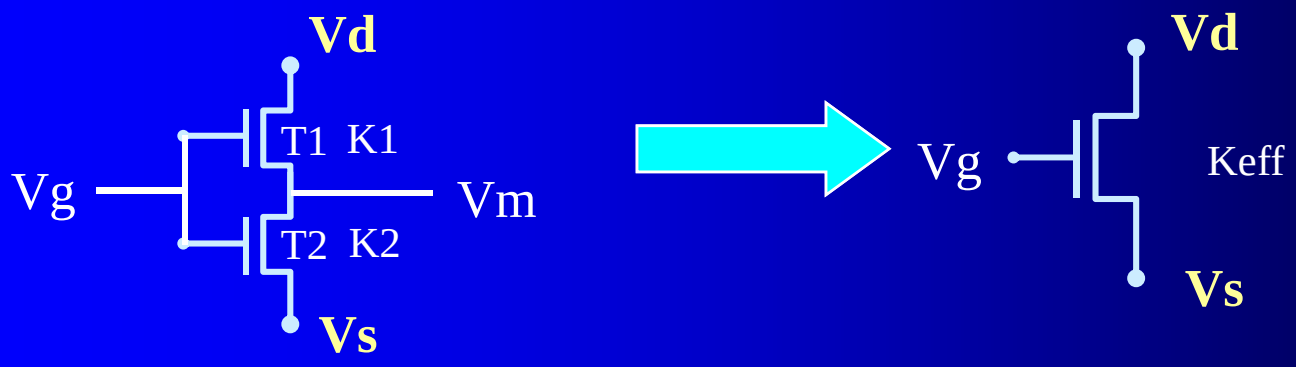




MOS管的串、并联特性

晶体管的驱动能力是用其导电因子k来表示的，k值越大，其驱动能力越强。多个管子的串、并情况下，其等效导电因子应如何推导？

一、两管串联：

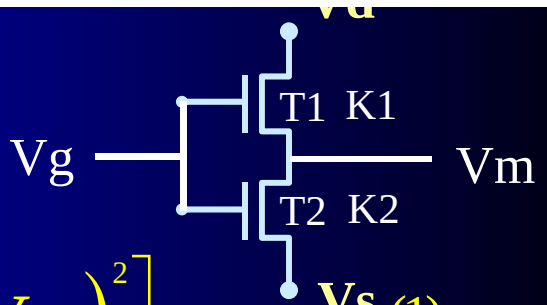


$$I_{DS} = K[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^{\,2}]$$

$$I_{DS} = K[(V_{GS} - V_{TH})^2 + 2(V_{GS} - V_{TH})V_{DS} - V_{DS}^{\,2} - (V_{GS} - V_{TH})^2]$$

$$I_{DS} = K[(V_{GS} - V_{TH})^2 - (V_{GS} - V_{TH} - V_{DS})^2]$$

设：Vt相同，工作在线性区。



$$I_{DS1}=K_1\left[\left(V_G-V_M-V_T\right)^2-\left(V_G-V_T-V_D\right)^2\right]\text{-----}(1)$$

$$I_{DS2}=K_2\left[\left(V_G-V_S-V_T\right)^2-\left(V_G-V_T-V_M\right)^2\right]\text{------}(2)$$

$$\because I_{DS1}=I_{DS2}$$

$$\therefore\left(V_G-V_M-V_T\right)^2=\frac{K_2}{K_1+K_2}\left(V_G-V_S-V_T\right)^2+\frac{K_1}{K_1+K_2}\left(V_G-V_T-V_D\right)^2$$

将上式代入（1）得：

$$I_{DS1}=\frac{K_1K_2}{K_1+K_2}[\left(V_G-V_S-V_T\right)^2-\left(V_G-V_T-V_D\right)^2]\text{-----}(3)$$

$$I_{DS}=K_{eff}[\left(V_G-V_S-V_T\right)^2-\left(V_G-V_T-V_D\right)^2]\text{------}(4)$$

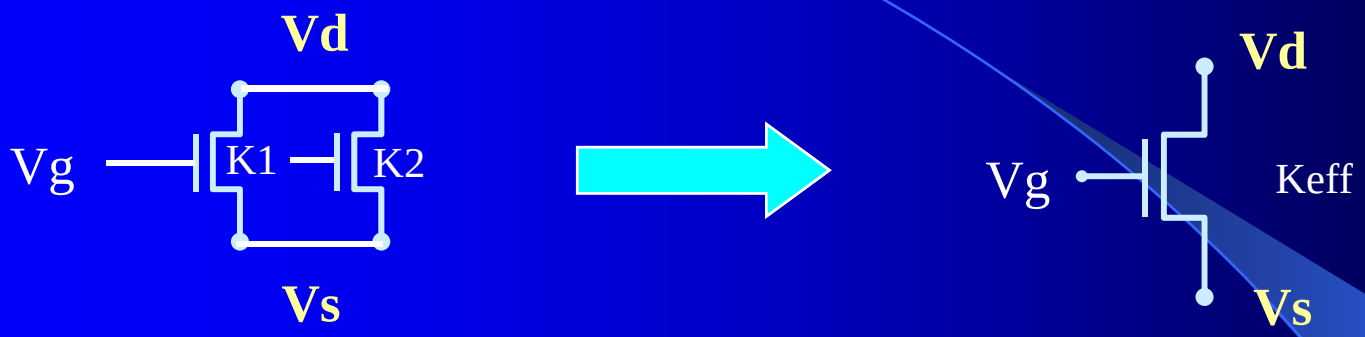
比较（3）（4）得：

$$K_{eff} = \frac{K_1 K_2}{K_1 + K_2}$$

同理可推出N个管子串联使用时，其等效增益因子为：

$$K_{eff} = \frac{1}{\sum_{i=1}^{N} \frac{1}{K_i}}$$

二、两管并联：



$$I_{DS} = I_{DS1} + I_{DS2} = (K_1 + K_2)[(V_G - V_T - V_S)^2 - (V_G - V_T - V_D)^2]$$

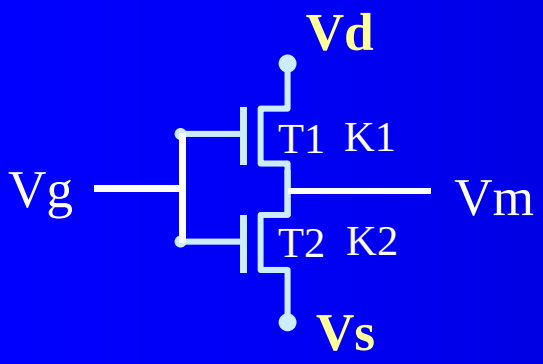
$$I_{DS} = K_{eff}[(V_G - V_T - V_S)^2 - (V_G - V_T - V_D)^2]$$

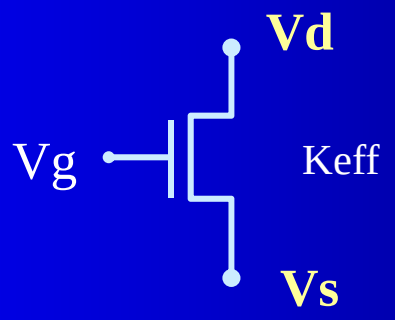
$$\therefore K_{eff} = K_1 + K_2$$

同理可证，N个Vt相等的管子并联使用时：

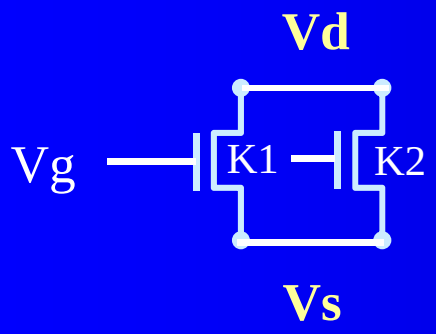
$$K_{eff} = \sum_{i=1}^{N} K_i$$

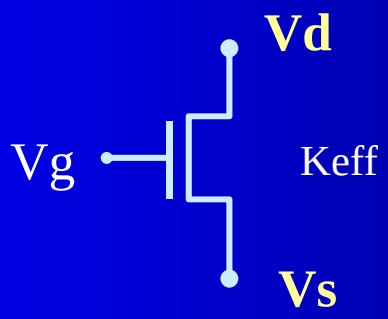
MOS管的串、并联特性





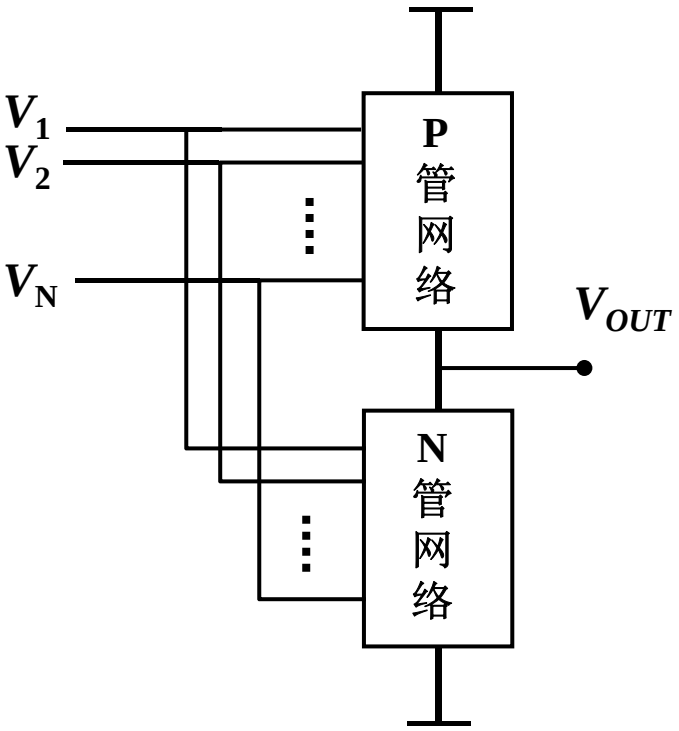
$$K_{eff} = \frac{K_1 K_2}{K_1 + K_2} \qquad K_{eff} = \frac{1}{\sum_{i=1}^{N} \frac{1}{K_i}}$$



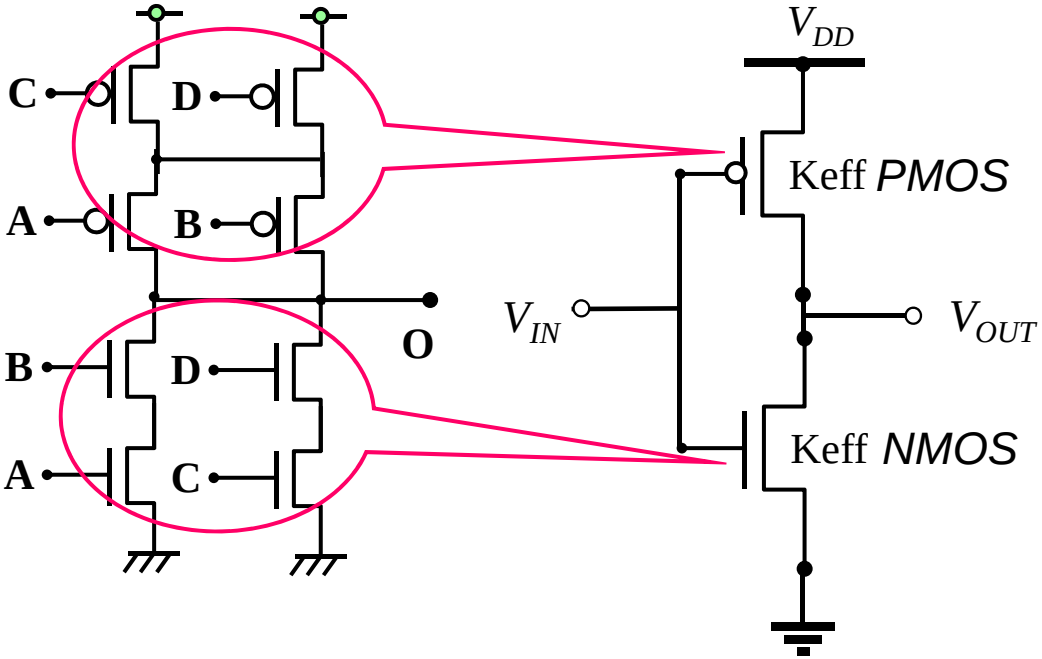


$$K_{eff} = K_1 + K_2 \qquad K_{eff} = \sum_{i=1}^{N} K_i$$

组合逻辑电路管子尺寸的设计



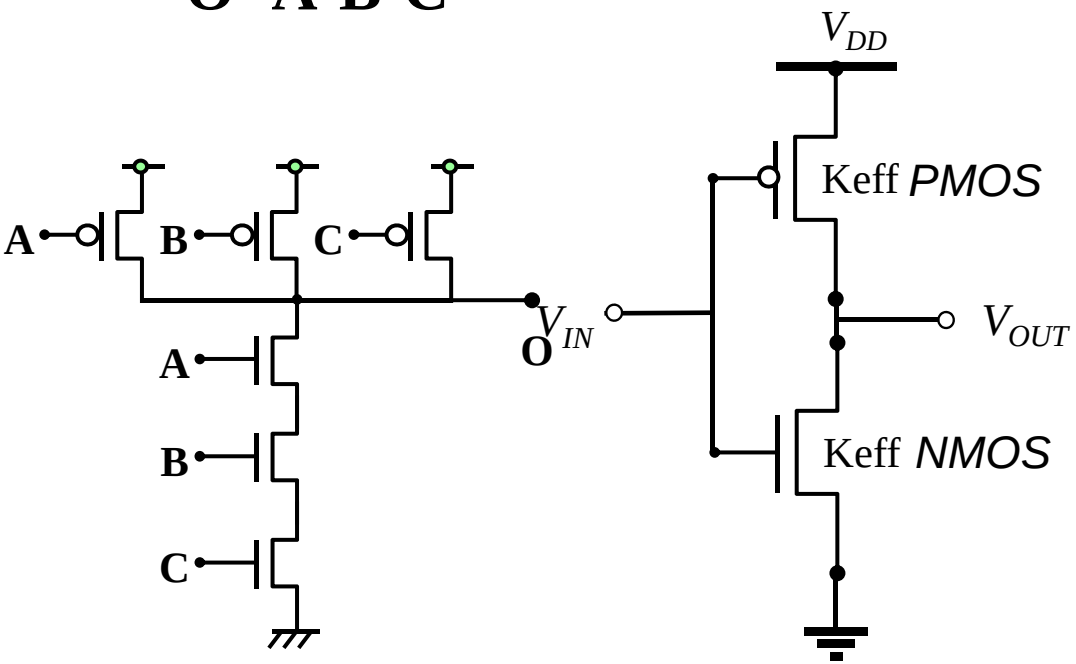
$$O=\overline{A\cdot B+C\cdot D}$$



CMOS组合逻辑电路的管子尺寸应如何设计

组合逻辑电路输入信号对驱动能力的影响

$$O=\overline{A\cdot B\cdot C}$$



假设：**P**网的等效导电系数为K_{Peff}

N网的等效导电系数为K_{Neff}

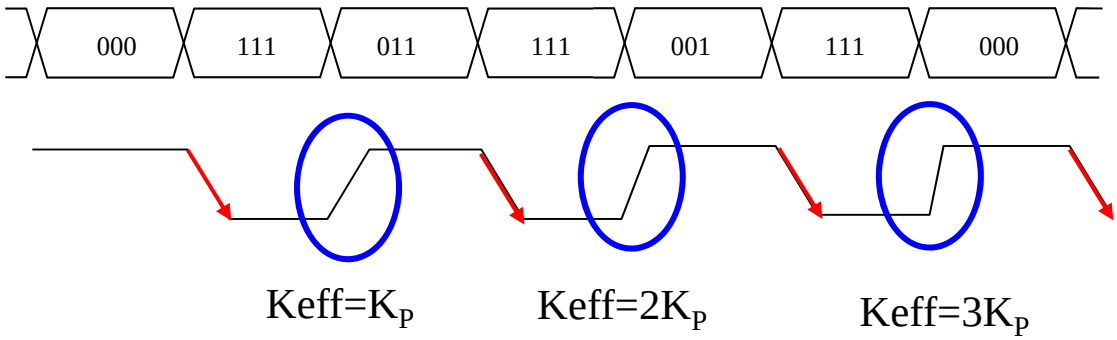
构成电路的所有**P**管具有相同导电系数K_P

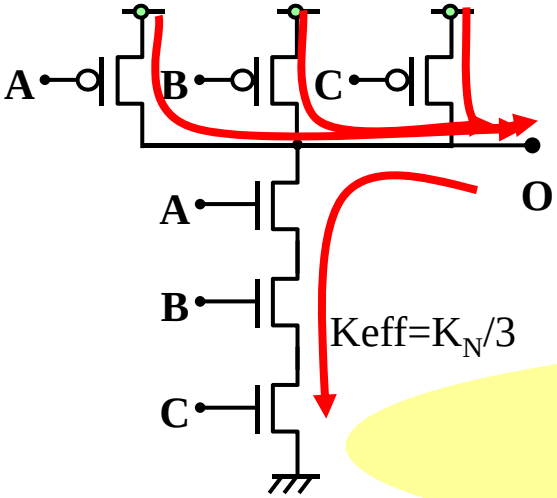
构成电路的所有**N**管具有相同导电系数K_N

输入信号			有效导通		等效导电因子	V_{OUT}
A	B	C	P管	N管		
0	0	0	3	0	$3K_p$	1
0	0	1	2	0	$2K_p$	1
0	1	0	2	0	$2K_p$	1
1	0	0	2	0	$2K_p$	1
0	1	1	1	0	K_p	1
1	0	1	1	0	K_p	1
1	1	0	1	0	K_p	1
1	1	1	0	3	$K_N/3$	0

对应不同的输入组合，**P**网及**N**网的等效导电因子不同！

不同输入组合时输入输出波形的变化





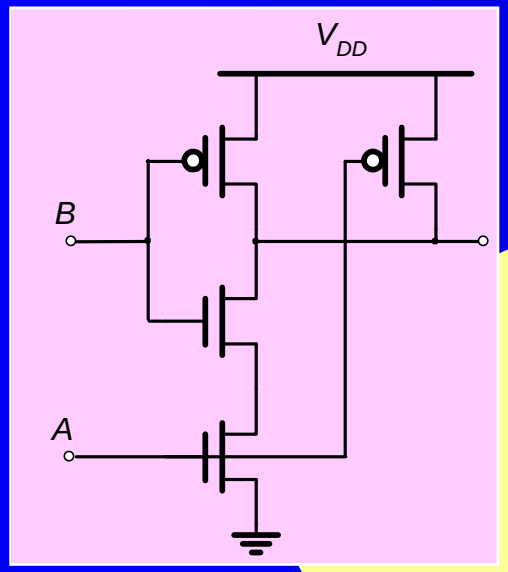
组合逻辑设计准则

上升时间和下降时间尽可能相同

输入信号组合不同时，上升时间不同

在最坏工作条件下，各个逻辑门的驱动能力要与标准反相器的特性相同。

与非门电路的驱动能力



$$X = \overline{a \bullet b}$$

在一个组合逻辑电路中，为了使各种组合门电路之间能够很好地匹配，各个逻辑门的驱动能力都要与标准反相器相当。即在最坏工作条件下，各个逻辑门的驱动能力要与标准反相器的特性相同。

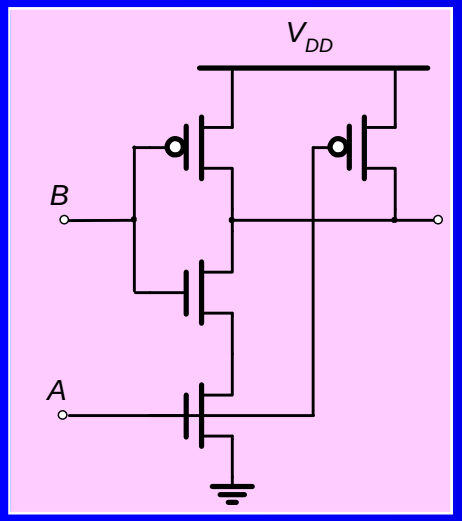
设：标准反相器的导电因子为Kn=Kp，

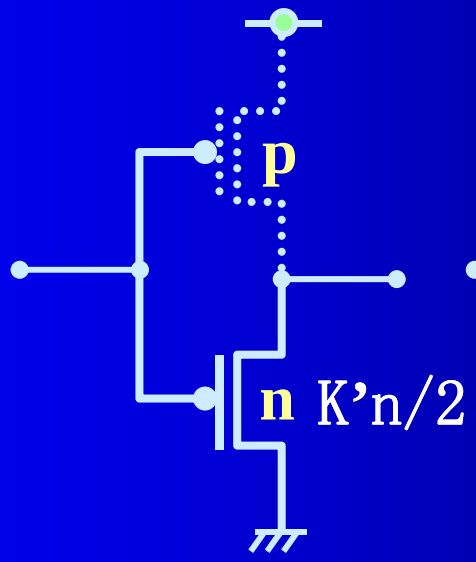
逻辑门：Kn1=Kn2=K'n　　Kp1=Kp2=K'p

(1) **a，b=1，** 1时，下拉管的等效导电因子：Keffn=K’n/2

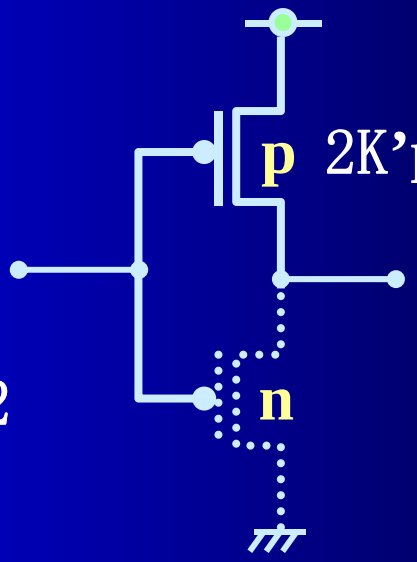
(2) a，b=0，0时，上拉管的等效导电因子：Keffp=2K’p

(3) a，b=1，0或0，1时，上拉管的等效导电因子：Keffp=K’p

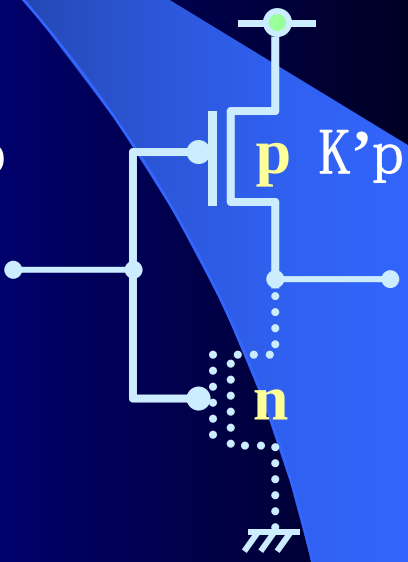




两个N管
串联



两个P管
并联



1个P管
工作

综合以上情况，在最坏的工作情况下，即：（1）、（3），应使：

Keffp=K’p=Kp

Keffn=K’n/2=Kn

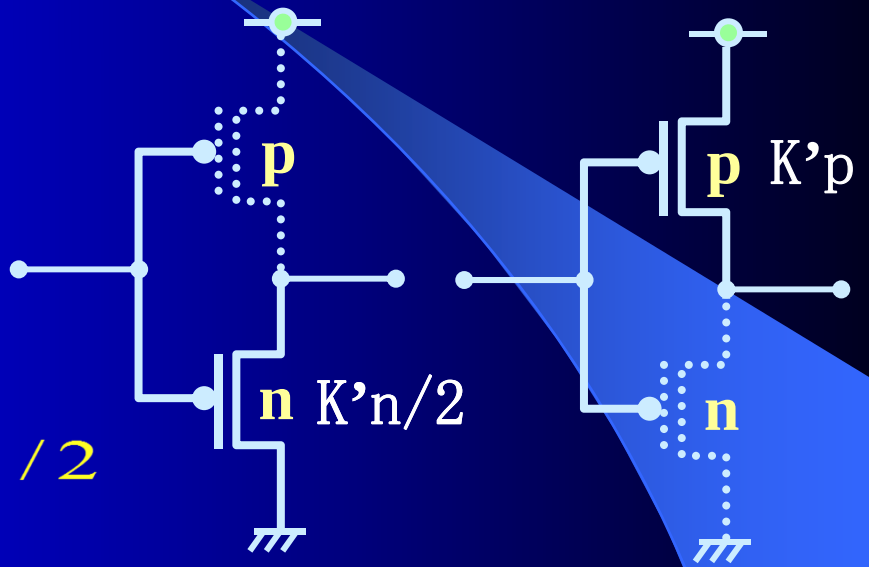
$$\because K = \mu C_{ox}(\frac{W}{L})$$

$$K_p = K_n$$

$$K_n^{'}/2 = K_p^{'}$$

$$\therefore \mu_p C_{ox}(\frac{W}{L})_p^{'} = \mu_n C_{ox}(\frac{W}{L})_n^{'}/2$$

$$\frac{W_p^{'}}{W_n^{'}} = \frac{\mu_n}{2\mu_p} \approx 0.5 \times 2.5 = 1.25$$

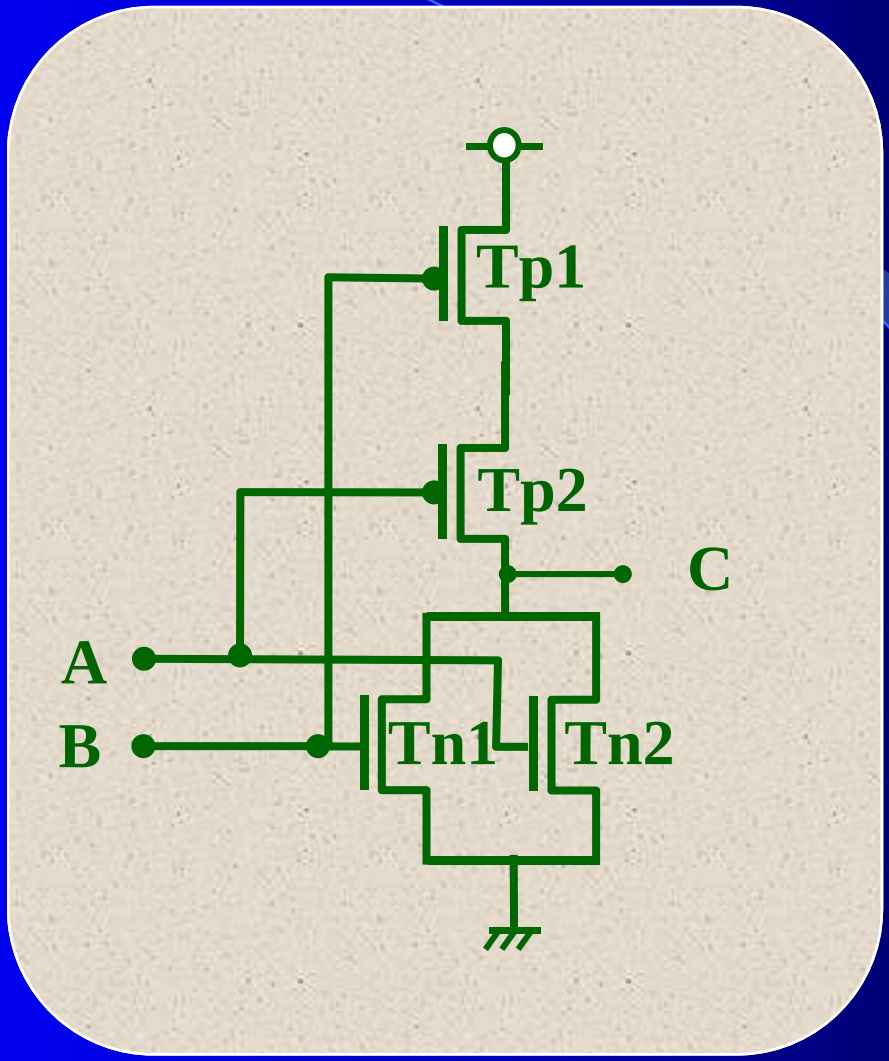


两个N管串联

1个P管工作

即要求p管的沟道宽度比n管大1.25倍以上。

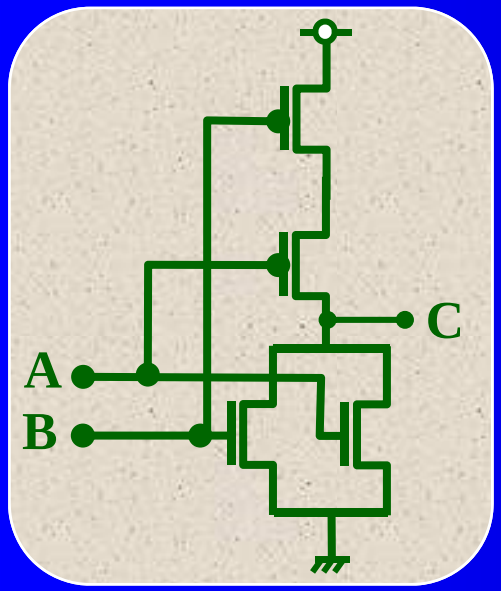
二、或非门：$X = \overline{a + b}$

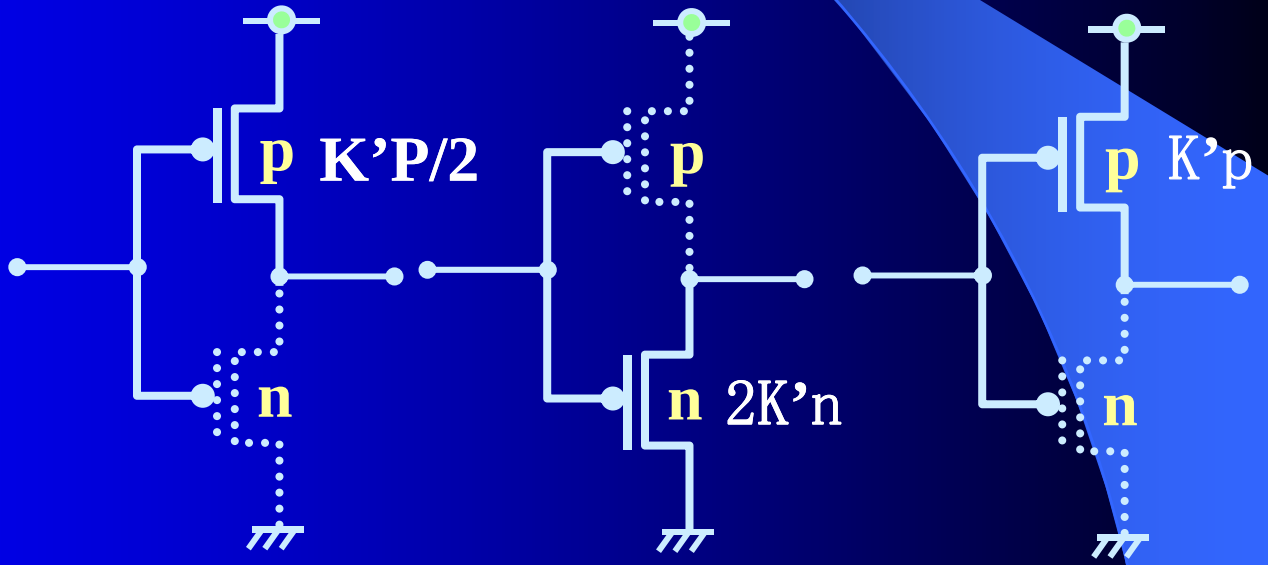


(1)当a，b=0，0 时，上拉管的等效导电因子：Keffp=K’p/2

(2)当a，b=1，1时，下拉管的等效导电因子：Keffn=2K’n

(3)当a，b=1，0或0，1时，下拉管的等效导电因子：Keffn=K’n





综合以上情况，在最坏的工作情况下，即：（1）、（3），应使：

Keffp=K’p/2=Kp

Keffn=K’n=Kn

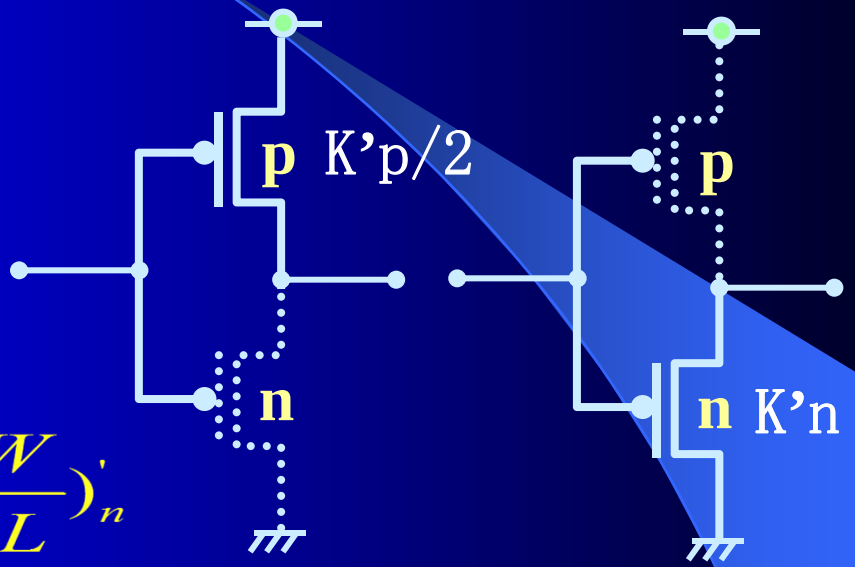
$$\because K = \mu C_{ox}(\frac{W}{L})$$

$$K_p = K_n$$

$$K_p'/2 = K_n'$$

$$\therefore \mu_p C_{ox}(\frac{W}{L})_p'/2 = \mu_n C_{ox}(\frac{W}{L})_n'$$

$$\frac{W_p'}{W_n'} = \frac{2\mu_n}{\mu_p} \approx 2 \times 2.5 = 5$$



两个N管
串联

1个P管
工作

即要求p管的沟道宽度比n管大5倍以上。

作　业

1.画出$O=\overline{A\cdot B+C\cdot D}$的CMOS组合逻辑门电路 。

2.计算题1复合逻辑门的驱动能力,为了保证最坏工作条件逻辑门的驱动能力要与标准反相器的特性相同,P管和N管的尺寸应如何选取。