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研发、设计、测试

一种可测性分析的新方法

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摘要 提出一种基于时序泰勒展开图（TTED）的VLSI高层可测性分析（TA）新方法，以时序泰勒展开图（TTED）为关键敏化路径建模，建立起确定性和概率性故障的统一表示模型。利用符号变量获取线路的敏感性，并且考虑电路的单敏化和多敏化情况，进行电路的可测性计算和分析，取得了较好的效果，实验证实了该方法的有效性。

关键词 超大规模集成电路（VLSI） 可测性 敏化方程 时序泰勒展开图

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New method of testability analysis

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Abstract

This paper proposes a VLSI high-level testability analysis（TA） new approach HLTA-TTED based on Timed Taylor Expansion Diagram（TTED），which models the critical sensitization path with TTED and establishes a unique representation model of certainty and probability failure.The line's sensitization is obtained by using the symbolic variable.Considering the case of single sensitization and multi-sensitization of the circuit，this paper computes and analyzes the testability of the circuit.A good result is obtained at last，the experiment confirms the approach's effectiveness.

Key words Very Large Scale Integrated circuits（VLSI） testability sensitization equation Timed Taylor Expansion Diagram（TTED）

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