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新型高速低功耗CMOS动态比较器的特性分析

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摘要: 为了降低sigma-delta模数转换器功耗, 针对应用于sigma-delta模数转换器环境的UMC 0.18 μm 工艺, 提出1种由参考电压产生电路、预放大器、锁存器以及用作输出采样器的动态锁存器组成的新型高速低功耗的CMOS预放大锁存比较器。该比较器中输出采样器由传输门和2个反相器组成, 可在较大程度上减少该比较器的功耗。电路采用标准UMC 0.18 μm 工艺进行HSPICE模拟。研究表明: 该比较器在1.8 V电源电压下, 分辨率为8位, 在40 MHz的工作频率下, 功耗仅为24.4 μW , 约为同类比较器功耗的1/3。

关键字: 预放大锁存比较器; sigma-delta ADC; 输出采样器; CMOS工艺

Characteristic analysis of a new high-speed and low-power CMOS dynamic comparator

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Abstract: To reduce power dissipation of a sigma-delta analog-to-digital converter, a new high-speed and low-power dissipation CMOS preamplifier-latch comparator, which is suitable for use in a sigma-delta analog-to-digital converter, was presented in CMOS 0.18 μm technology. The comparator consists of a reference voltage generation circuit, a preamplifier and a latch stage followed by a dynamic latch that operates as an output sampler. The output sampler circuit consists of a full transmission gate(TG) and two inverters. The use of this sampling stage results in the reduction in the power dissipation of the high-resolution comparator. Hspice simulations of the proposed circuit in a UMC 0.18 μm standard CMOS technology operating at supply voltage of 1.8 V was made. The results show that the resolution is 8 bit and the power dissipation is only 24.4 μW at 40 MHz. The power dissipation is about 1/3 of that of the similar comparators.

Key words: preamplifier-latch comparator ; sigma-delta ADC; output sampler; CMOS process

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