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论文

基于VHDL的正交编码脉冲电路解码计数器设计

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摘要：

针对正交编码脉冲电路脉冲(quadrature encoder pulse, QEP)的解码和计数的问题，给出了QEP解码计数器的解决方案.本方案在复杂可编程逻辑器件(complex programmable logic device, CPLD)中使用VHDL(VHSIC hardware description language)实现语言硬件编程.整个解码计数器设计分为脉冲边沿检测器，计数脉冲和计数方向发生器，上下行计数器三部分，成功的解决了由传感器抖动引起频繁换向时准确计数的问题.该解决方案使用Altera公司的Quartus II软件进行设计并进行了仿真分析，最后给出了基于此技术的机床数显表的应用实例来说明此技术的可行性和柔性.

关键词： 正交编码脉冲 解码 VHDL硬件语言编程 复杂可编程逻辑器件

Design of a QEP decode counter based on VHDL

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Abstract:

To solve problems in decoding and counting of Quardrature Encoder Pulse (QEP), a design of a QEP decode counter was presented. VHSIC hardware description langurage (VHDL) was used as the programming language, which was implemented in a complex programmable logic device (CPLD). The whole structure of this design includes three parts: edge pickers, pulse/direction generator and up/down counter. By using this structure, the counting accuracy in a dithering case was successfully guaranteed. Altera Quartus II was used for design as well as simulation analysis. The application in Digital Readout for machine tools was given to improve the feasibility and flexibility.

Keywords: quadrature encoder pulse (QEP) decoder VHSIC hardware description language (VHDL) complex programmable logic device (CPLD)

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