1. What is the definition of sheet resistance in semiconductors and why do people want to define such a physical quantity?
(5%)

2. At what energy position does the intrinsic Fermi lie? Please derive its explicit expression.
(10%)

3. (a) For an n-type semiconductor with a donor concentration of 10^{16} cm^{-3}, plot the carrier concentration as a function of inverse temperature (1/T).
(b) Explain the reasons for this behavior in the three different regions.
(10%)

4. (a) Draw the energy band diagram for a metal to n-type semiconductor junction. Assume that the work function of the metal is larger than that of the semiconductor, that is: $q\phi_m > q\phi_s$. $q\phi_m$ is the work function of the metal and $q\phi_s$ is the work function of the semiconductor. $q\chi$ is electron affinity and q is electronic charge. Find out the Schottky barrier height and the contact potential.
(b) Draw similar energy band diagram for a metal to p-type semiconductor junction. Assume $q\phi_m < q\phi_s$. Find out the Schottky barrier height and the contact potential.
(15%)

5. Three npn bipolar junction transistors (BJT) are identical except that BJT#2 has a base region width (W) twice as long as BJT#1, and BJT#3 has a base region doping concentration (N_A) twice as heavy as BJT#1. All other device structure parameters are identical for these three BJTs and the same forward active bias. Answer the following questions with a brief and clear mathematical reasons. NO credit will be given for answer without explanation.

(a) Which one has the highest collector current? (4%)
(b) Which one has the highest emitter injection efficiency? (3%)
(c) Which one has the highest base transport factor? (3%)
(d) Which one has the lowest punchthrough voltage? (3%)
(e) Which one has the highest common emitter current gain? (3%)
(f) Which one has the highest collector junction capacitance? (3%)
(g) Which one has the highest Early voltage? (3%)
(h) Which one has the largest base transit time? (3%)

6. In CMOS ICs, the n+ polysilicon is often used for local interconnection. The n+ ploysilicon layer forms parasitic MOS field transistors over the field oxides. Assume the p-well is uniformly doped at N_{al} and the doping level is the same under the field oxides and the gate oxides. The gate oxide thicknesses for both NMOSFET and PMOSFET are (t_{oxf}) 100 Å and the threshold voltage, (V_{Tf}), 0.5V for the normal NMOS transistors. Use appropriate approximation in the answering these questions.

(a) Assume the maximum voltage on the n+ polysilicon gate is 20V, estimate the minimum field oxide thickness needed to prevent turning on the parasitic MOS field transistors. (5%)

(b) Assume field oxide thickness is fixed at 2000 Å, what should the doping level under the field oxide be in relation to N_{al} to meet the requirement in (a). (5%)

(c) If only n+ poly-silicon can be implemented in a CMOS process, estimate the threshold voltage, V_{TP}, of the pMOSFETs, assuming n-well substrate doping level, $N_{dl}=N_{al}$ (5%)

(d) The V_{TP} of the pMOSFETs is generally found to be at an unacceptable level, a channel implant of acceptor impurities is one solution change the V_{TP} and form a buried channel device. Can you plot the energy band diagram of a buried channel pMOSFET at zero-bias?(5%)

(e) Discuss the advantages and disadvantages of a buried channel MOSFET. (5%)

7.

(a) Describe how sub-threshold swing of a MOSFET is defined. (5%)

(b) If the substrate doping increases, how will the sub-threshold swing change? Explain why.(5%)