



## 考虑寄生参数的集成电路ESD损伤仿真方法

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## ESD damage simulation of integrated circuits by the consideration on parasitic parameters

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摘要

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**摘要** 在传统的基于设计电路的ESD (Electro-Static Discharge)损伤仿真中,通常不考虑版图物理结构的影响,其仿真结果往往与实际损伤情况出现较大偏差,因此提出了一种考虑版图设计中寄生参数的集成电路ESD损伤的仿真方法.首先给出了仿真应用的具体分析流程.然后按照经验公式提取法明确了各种寄生参数的计算模型.最后,以集成运算放大器LM741为例,对其进行了ESD损伤模拟,再通过击打实验、失效定位与电性能测试,结果表明:仿真与实验结果具有较好的一致性,验证了该方法的有效性.

**关键词:** ESD损伤 版图结构 寄生参数 电路仿真 可靠性设计

**Abstract:** In the traditional electro-static discharge (ESD) damage simulation based on logic circuit, the influence of layout was not taken into account as usual, and there was larger deviation between the results of simulation and the actual damage, so a new simulation method of ESD damage for integrated circuits was presented by the consideration for parasitic parameters extraction in layout. Firstly the specific simulation process in the application was given. Then the models of kinds of parasitic were defined according to empirical parameter extraction method. Lastly the ESD damage simulation for integrated operational amplifier LM741 as case study was carried out. According to zap test, failure location and electrical performance testing, the results showed have much consistency in simulation and experiment, and the validity of the simulation method is finally verified.

**Keywords:** ESD damage layout parasitic parameter circuit simulation design for reliability

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