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论文

# 一种星簇双环片上网络拓扑结构

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摘要：

随着半导体工艺的不断发展和芯片中所包含的IP核数目的增加，片上系统的互连结构对系统性能和面积具有极大的影响．为了减少节点度、减少链路和重用路由器节点，提出了一种规则的片上互连网络——星簇双环 (Star-Cluster Double-Loop，SCDL(2m))拓扑结构，该拓扑结构具有4m个节点并且每个节点连接3个相邻节点和4个IP核．SCDL(2m)是一种拓扑结构简单、平面的、对称的并且具有良好扩展性的互连网络．SCDL(2m)互连网络节点采用一种新的约翰逊编码方法，使得路由算法简单高效．在不同负载和不同节点数量情况下，对SCDL(2m)，Cluster-Ring和Cluster-Mesh网络的平均通讯延迟和平均吞吐量进行了模拟分析，结果表明SCDL(2m)互连网络较好的平衡了网络性能和成本，是一种简单高效的片上互连网络．

关键词： 片上系统 片上网络 网络拓扑 路由算法

## Star-cluster double-loop topology for the network-on-chip

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Abstract:

With the feature size of semiconductor process reduced and IP(Intellectual Properties) cores increased, interconnection network architectures on the chip have a great influence on the performance and area of System-on-Chip(SoC) design. Focusing on decreasing node degrees, reducing links and reusing the router node, a regular Network-on-Chip(NoC) architecture, named the Star-Cluster Double-Loop(SCDL (2m)) interconnection network, is proposed. The topology of SCDL(2m) is simple, planar, symmetric and scalable in architecture, and it has 4m nodes. Each node connects three adjacent nodes and four IP cores. The nodes of SCDL(2m) adopt the Johnson coding scheme that can make the design of routing algorithm simple and efficient. The SCDL(2m) is compared with Cluster-Ring and Cluster-Mesh by simulation and analysis, both under a uniform load and under more realistic load assumptions in several network size scenarios. The results show that the SCDL(2m) topology is a good trade-off between performance and cost. It is a better topology for NoC.

Keywords: system-on-chip network-on-chip network topology routing algorithms

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参考文献：

［1］Benini L, Micheli G D. Networks on Chip: a New Paradigm for Systems on Chip Design ［C］//Proceedings of Design Automation and Test in Europe Conference and Exhibition. Paris: IEEE, 2002: 418-419.

［2］Horowitz M, Dally W. How Scaling Will Change Processor Architecture［C］//IEEE International Solid-State Circuits Conference. San Francisco: IEEE, 2004: 132-133.
［3］Dally W J, Towles B. Route Packets, Not Wires: On-chip Interconnection Networks［C］//Proceedings of Design Automation Conference. Las Vegas: IEEE, 2001: 684-689.
［4］徐阳扬, 周端, 杨银堂, 等. 非对称GALS系统异步接口设计［J］. 西安电子科技大学学报, 2007, 34(2): 294-297.
Xu Yangyang, Zhou Duan, Yang Yintang, et al. Unsymmetrical Interface Design in GALS［J］. Journal of Xidian University, 2007, 34(2): 294-297.
［5］Ye T. On-chip Multiprocessor Communication Network Design and Analysis［D］. California: Stanford University, 2003.
［6］Hu J, Marculescu R. Energy-and Performance-aware Mapping for Regular NoC Architectures［J］. IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24(4): 551-562.
［7］Salminen E, Kulmala A, Hamalainen T D. Survey of Network-on-Chip Proposals［R/OL］.［2008-09-12］. http://www.ocpip.org/socket/whitepapers/.
［8］Salminen E, Kulmala A, Hamalainen T D. On Network-on-chip Comparison［C］//10th Euromicro Conference on Digital System Design Architectures, Methods and Tools. Lübeck: IEEE, 2007: 503-510.
［9］Saneei M, Afzali-Kusha A, Navabi Z. Low-power and Low-latency Cluster Topology for Local Traffic NOCs［C］//Proceedings of IEEE International Symposium on Circuits and Systems. Island of Kos: IEEE, 2006: 1-5.
［10］Jayasimha D N, Zafar B, Hoskote Y. On-Chip Interconnection Networks: Why They are Different and How to Compare Them［EB/OL］.［2008-09-12］. blogs. intel.com/research/terascale/.
［11］Duato J, Yalamanchili S, Ni L. Interconnection Networks: an Engineering Approach［M］. Netherland: Elsevier Science, 2003.
［12］Bononi L, Concer N. Simulation and Analysis of Network on Chip Architectures: Ring,Spidergon and 2D Mesh［C］//Proc of the Design, Automation and Test in Europe(DATE). Munich: IEEE, 2006: 54-159.

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1．杨帆;邱智亮;刘增基;严敬 .高速交换网络中基于综合优先级计算的调度及路由算法[J]. 西安电子科技大学学报, 2007,34(5): 702-707
2．王静1;刘景美1;王新梅1;袁荣亮2;刘向阳3 .一种网络编码的多播路由算法[J]. 西安电子科技大学学报, 2008,35(1): 71-75
3．米志超;鲍民权;郑少仁.一种基于多跳Ad Hoc网络的路由协议的设计与实现[J]. 西安电子科技大学学报, 2001,28(6): 707-711
4．秦浩;张SHI;刘增基.一种非对称OBS网络中的路由算法[J]. 西安电子科技大学学报, 2006,33(4): 568-571
5．暂时无作者信息.基于遗传策略的实时多点传送路由算法[J]. 西安电子科技大学学报, 2000,27(2): 215-219
6．翟艳;杨银堂;朱樟明;王帆.一种基于SOC应用的Rail-to-Rail运算放大器IP核[J]. 西安电子科技大学学报, 2005,32(1): 112-115
7．王长山1;牛继云1;顾华玺2;柯楚3 .一种直连网络智能路由算法[J]. 西安电子科技大学学报, 2007,34(4): 532-537
8．尚玉玲;李玉山.面向测试的SOC核间互连网络约简算法[J]. 西安电子科技大学学报, 2009,36(5): 871-876+956

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