2003年微电子学研究所发表的学术论文

一、器件研究室

一种集成PCR与CE的生物芯片的设计研究

季旭，刘理天

半导体技术，2003年第8期

本文阐述了一种集成PCR反应室与CE管道的生物芯片的研究和设计工作。研发目的是实现样品扩增、电泳分离和紫外光检测3个生物分析检测过程的单片集成。我们为这种DNA生物芯片设计了PCR反应池及其加热控制系统、毛细管电泳管道和配备即时测温功能的辅助电路系统（PCB板），并且完成了芯片的版图设计以及工艺方案及具体工艺参数设计。整个系统可以基本实现一个小型DNA检测实验室的功能。

The design of a biochip integrated with PCR and CE

Ji Xu, Liu Li-tian

Semiconductor Technology No. 8, 2003

We have designed a biochip integrated with PCR chamber and CE pipelines. The design purpose of this biochip is to integrate PCR reaction, CE separation and ultraviolet radiation inspection in only one chip. We also designed a PCB integrated with the PCR control system and the temperature-detective system, drew the layout, designed the process of the biochip and selected the process characters. The whole system basically realizes the functions of laboratory on a chip.

一种集成PCR反应室与CE的生物芯片的研究

季旭，刘理天

仪器仪表学报，2003年第4期增刊

生物芯片是便携式生物化学分析仪器的核心技术。通过基于MEMS的微加工工艺技术在硅、玻璃等介质上形成生物化学处理所需的微型结构，从而使成千上万个与生命相关的信息紧密有机地集成在一块芯片上。运用生物芯片可进行生命科学和医学中所涉及的各种生物化学反应，从而达到对基因、抗原和活体细胞等进行测试分析的目的。本文阐述了一种集成了PCR（Polymerase Chain Reaction 聚合酶链式反应)反应室与CE （Capillary Electrophoresis毛细管电泳） 管道的生物芯片的研究和设计工作，研发这款生物芯片的目的是实现样品扩增、电泳分离和紫外光检测3个生物分析检测过程的单片集成。我们为这种DNA生物芯片设计了PCR反应池及其加热控制系统、毛细管电泳管道和配备即时测温功能的辅助电路系统（PCB板），并且完成了芯片的版图设计以及工艺方案及具体工艺参数设计。整个系统可以基本实现一个小型DNA检测实验室的功能。设计的这款生物芯片用途有DNA测序，DNA突变检测和识别不明微生物。

The design of a biochip integrated with PCR chamber and CE

Ji Xu, Liu Litian

CHINESE JOURNAL OF SCIENTIFIC INSTRUMENT，No.4 supplement，2003

Biochip is the core technology of handy biochemical instruments. We can inspect DNA, antigen and lively cells in some biochemical reaction with these tools which are fabricated by using MEMS technologies to mold micro construct on such materials, like silicon, glasses and plastic.

We have designed a biochip integrated with PCR chamber and CE pipelines. The design purpose of this biochip is to integrate PCR reaction, CE separation and ultraviolet radiation inspection in only one chip. We also designed a PCB integrated with the PCR control system and the temperature-detective system, drew the layout by using L-edit software, designed the process of the biochip and selected the process characters. The whole system is basically realizing functions of laboratory on a chip. It can be used in measuring DNA sequence，inspecting DNA mutation and identifying unclear microbe.

基于PZT压电薄膜的微麦克风

杨轶，张林涛，张宁欣，伍晓明，王海宁，蔡坚，任天令，刘理天

第八届全国敏感元件与传感器学术会议, Proc. STC’03, pp. 429-431

采用Sol-Gel方法制备了高品质的硅基PZT薄膜，利用微机械加工技术，实现了基于PZT压电薄膜的微麦克风。对芯片级和封装后的压电微麦克风进行了测试，测试表明本文制备的微麦克风具有可靠性高，频带宽的特点

Miniature Microphone based on PZT Piezoelectric Thin Films

Yi Yang, Lin-Tao Zhang, Ning-Xin Zhang, Xiao-Ming, Hai-Ning Wang, Jian Cai, Tian-Ling Ren, Li-Tian Liu

The 8th Sensor Technology Conference, Proc. STC'03, pp. 429-431

A novel PZT-based micromachined miniature microphone has been proposed, fabricated and tested. High quality and silicon-based PZT thin films have been prepared using an improved Sol-Gel method. The wafer-level and post-packaging test shows that the fabricated microphone has the advantages of high reliability and broadband response.

压电薄膜悬臂梁结构的建模和性能模拟

杨轶，张林涛，张宁欣，伍晓明，任天令，刘理天

第八届全国敏感元件与传感器学术会议, Proc. STC'03, pp. 135-138

用ＡＮＳＹＳ软件建立了压电薄膜悬臂梁结构的有限元模型，对悬臂梁进行了结构静力分析、模态分析，计算出了悬臂梁的谐振频率和振型。对基于压电薄膜悬臂梁结构的微麦克风和扬声器进行了灵敏度计算和谐波响应分析。

Modeling And Analysis of Piezoelectrically Actuated Cantilever

Yi Yang, Lin-Tao Zhang, Ning-Xin Zhang, Xiao-Ming, Tian-Ling Ren, Li-Tian Liu

The 8th Sensor Technology Conference, Proc. STC'03, pp. 135-138

This article describes the modeling and analysis of a piezoelectrically actuated cantilever using a FEA tool – ANSYS. Static analysis and modal analysis of the cantilever has been performed to obtain the vertical displacement under a DC voltage and calculate the resonance frequencies and mode shapes. The sensitivity and harmonic response of a cantilever-based integrated microphone and microspeaker are also analyzed.

集成铁电器件中的关键工艺研究

杨轶，张宁欣，任天令，刘理天

首届全国信息获取与处理学术会议

仪器仪表学报, Vol. 24, No. 4, 2003, pp. 192-193

本文对集成铁电器件中的关键工艺进行了研究，采用改进的溶胶－凝胶（Sol-Gel）法制备了高品质、（110）择优取向的锆钛酸铅（PZT）铁电薄膜，成功的利用离子束刻蚀（IBE）、反应离子刻蚀（RIE）和湿法腐蚀方法对PZT薄膜进行了刻蚀加工，采用正胶剥离和干法刻蚀工艺实现了金属铂（Pt）电极图形，为集成铁电器件的实现提供了良好的工艺基础。

Study on the Key Processes of Integrated Ferroelectric Device

Yi Yang, Ning-Xin Zhang, Tian-Ling Ren, Li-Tian Liu

Chinese Journal of Scientific Instrument, Vol. 24, No. 4, 2003, pp. 192-193

Key processes of integrated ferroelectric devices based on silicon have been studied. High quality and (110) preferential oriented ferroelectric thin films, lead zirconate titanate (PZT), have been prepared using an improved sol-gel method. PZT thin films have been successfully patterned by ion beam etching (IBE), reactive ion etching (RIE) and wet etching. The platinum electrodes have been well patterned by lift-off process and dry etching techniques.

压电微传声器的有限元分析

杨轶，张林涛，任天令，刘理天

首届全国信息获取与处理学术会议

仪器仪表学报, Vol. 24, No. 4, 2003, pp. 194-195

本文利用ANSYS软件建立了压电微传声器的有限元模型，对器件进行了结构静力分析、模态分析、谐波分析，计算模拟出微传声器的本征频率。通过模拟和分析，对压电传声器的设计参数进行了优化。对比表明，有限元分析的结果与解析方法以及实验结果相一致。

Analysis of a piezoelectric acoustic sensor using FEA method

Yi Yang, Lin-Tao Zhang, Tian-Ling Ren, Li-Tian Liu

Chinese Journal of Scientific Instrument, Vol. 24, No. 4, 2003, pp. 194-195

A piezoelectric acoustic sensor has been effectively studied using of the finite element analysis (FEA) tool – ANSYS. The device is composed of a Pt/PZT/Pt/SiO2/Si multi-layer membrane. Static and dynamic analysis of the micro-machined miniature acoustic sensor has been performed. It has been shown that ANSYS gives results comparable with those obtained from analytical methods and experiments. The device structure has been optimized and high performance can be realized.

MEMS的研究与应用

杨轶，张宁欣，张林涛，陈兢，任天令，刘理天

中国集成电路，No.53，2003，p22-25

本文介绍了MEMS的基本概念、基本特征和理论基础，并结合MEMS的发展史和制造技术，对MEMS的应用领域作了重点阐述，最后对MEMS的发展前景和产业化的挑战作了分析。

Micro-Electro-Mechanical-System Technology and Its Applications

Yi Yang, Ninxin Zhang, Lintao Zhang, Jing Chen, Tianling Ren, Litian Liu

China Integrated Circuit, No. 53, 2003, p22-25

The conception, characteristics and theory of MEMS are introduced in this paper. The discussion is focused on applications of MEMS, as well as its history and fabrication technologies. Finally the prospect and challenge to industrialization are analyzed.

基于MEMS技术的集成铁电硅微麦克风

伍晓明，杨轶，张宁欣，蔡坚，任天令，刘理天

中国集成电路，No. 53，p59-61, 2003

本文介绍了基于 MEMS技术的集成铁电式硅微麦克风的潜在应用、制备工艺、封装技术、测试方法。实验研究表明，这种与IC工艺相兼容的MEMS微麦克风工艺相对简单，性能易于控制，灵敏度可以达到15mV/Pa以上，有很大的发展前途。

MEMS-based Integrated Ferroelectric Microphone

Xiaoming Wu, Yi Yang, Ninxin Zhang, Jian Cai, Tianling Ren, Litian Liu

China Integrated Circuit, No. 53, p59-61, 2003

This paper introduces a Micro-electronic-mechanical System (MEMS) based integrated ferroelectric microphone, including its potential applications, fabrication process, packaging and test technology. The test results show that ferroelectric MEMS microphone is IC compatible, performance easy controlled, and with high sensitivity up to 15mV/Pa. This kind of MEMS microphone is very promising in the future.

硅基法布里-珀罗微腔的红光发射*

但亚平 姚永昭 王燕 岳瑞峰 刘理天

半导体学报，2003，24(S):60-64.

以PECVD为制备工艺，a-SiO2:H/a-Si:H为分布式布拉格反射镜的多层膜， a-SiCx:H为中间腔体发光材料，制备出垂直腔面的发光微腔。根据模拟结果确定了微腔的多层膜层数和排列顺序，并在250℃下制备出了这种微腔；将微腔样品分别在不同温度下进行退火，对退火前后的微腔进行了反射谱和荧光谱研究。结果表明，微腔能激射出波长为743nm、半高宽为9nm的荧光，在350℃退火后发光性能进一步提高，而450℃退火后，性能恶化。

Red light emission from Si-based Fabry-Perot Microcavities*

Dan Yaping, Yao Yongzhao, Wang Yan, Yue Ruifeng, Liu Litian

Chinese Journal of Semiconductors, v 24, n SUPPL., May, 2003, p 60-64

A microcavity prepared by PECVD is proposed in this paper. Its distributed Bragg reflectors are composed of periodically stacked a-SiO2:H/a-Si:H layers and the active layer is filled with a-SiCx:H. The structure of a microcavity is determined through simulating. In experiment a microcavity is prepared at 250℃ and annealed at different temperatures. Reflectance and PL spectra are recorded on as-deposited and annealed samples. It is indicated that the as-deposited sample performs well and even better after annealed at 300℃, however worse after annealed at 450℃.

一种新型硅基垂直腔面光发射器件的设计与模拟*

姚永昭 岳瑞峰 刘理天

STC'2003, 572~576

本文提出了一种新型硅基垂直腔面光发射器件结构。它采用等离子增强化学汽相淀积(PECVD)方法制备的非晶硅（或非晶氮化硅）/二氧化硅交替生长的多层薄膜结构为布拉格反射器（DBR），以夹在上下两个布拉格反射器之间的非晶碳化硅薄膜为中间发光层。通过设计与模拟，分析了DBR中薄膜生长顺序与层数对器件性能的影响。

Design and simulation of a novel Si-based Vertical Cavity Surface Light Emitting (VCSLE) device

Yao Yongzhao, Yue Ruifeng, Liu Litian

STC'2003, 572~576

A novel structure of Si-based Vertical Cavity Surface Light Emitting (VCSLE) device is proposed. The light emission a-SiC:H layer and the DRB stack which consists of a-Si (or a-SiNx)/a-SiO2 multifilms are both prepared by Plasma Enhanced Chemical Vapor Deposition (PECVD). The effect of multifilm preparation sequence and layer amount on the device performance is analyzed by design and simulation.

悬浮结构电感的模拟与制作

刘泽文，陈忠民，丁勇，刘理天，李志坚

STC'2003, 2003年11月16－18日，北京

本文分析了衬底对射频无源器件性能的影响，提出30μm空气隔离层的悬浮结构可以大大降低衬底损耗。通过模拟空气层隔离后的衬底损耗，简化了悬浮电感的电学模型，计算得到高Q值电感的优化尺寸结构。通过阳极氧化形成多孔硅牺牲层可以实现这种悬浮结构电感，利用SiO2作支撑膜，Al金属作线圈的结构材料，最后使用改进的TMAH溶液释放牺牲层。该制作工艺与CMOS工艺兼容。

Simulation and fabrication of a suspended inductor

Liu Zewen, Chen Zhongmin, Ding Yong, Liu Litian, Li Zhijian

STC'2003, Nov. 16-18, 2003, Beijing

The substrate effects to the passive device are analyzed. A 30μm suspended structures on the air can reduce greatly the substrate loss. The modeling with air gap is much more simple. The inductor structure is than optimized based on the simulation. The suspended inductor structure can be realized as the following steps: anodizing the silicon and forming a thick layer of porous silicon, oxide deposition on to the porous layer to be used as supporting membrane, aluminum structure fabrication and porous releasing with TMAH solution。The process is compatible with CMOS process.

用于一节倒立摆中的模糊控制算法及FPGA实现

王中大 靳东明

微电子学，Vol.33, No.1, Feb.2003:29-32.

本文将单变量推理单元SIRM（Single Input Rule Module）模糊控制算法，采用Xilinx 公司的FPGA实现，设计了以8 bit的数字模糊控制器为核心的数字电路控制系统，成功地实现了对硬件一节倒立摆的实时控制。倒立摆可以被控制在指定滑轨位置左右3厘米的区间内，偏离竖直方向小于3度。

FPGA implementation of Fuzzy Controlling on Inverted Pendulum

Wang Zhongda, Jin Dongming

Microelectronics ,Vol.33,No.1,Feb.2003: 29-32.

SIRM (Single Input Rule Module), a Fuzzy Controlling algorithm has been implemented by FPGA from Xilinx, and used to control a real inverted pendulum. The SIRM controller is an 8-bit digital controller that can balance the inverted pendulum well as was verified by experiment. The inverted pendulum can be balanced within 3 degree around the upright position with the cart be appointed to any position on the rail within 3 cm by the controller.

二维Ge岛成核早期阶段的动力学蒙特卡罗模拟

邓宁 肖鸿 陈培毅 李志坚

半导体学报，vol24,2003

本文采用动力学蒙特卡罗（Kinetic Monte Carlo）方法模拟了Si/Ge系统自组织生长Ge量子点过程中二维Ge岛成核的早期阶段。引入吸附原子导致的应力场对原子扩散的势垒进行了修正。研究了温度和应力场分布对二维Ge岛成核位置以及尺寸分布的影响，结果表明应力场对二维岛的成核具有决定作用，采用调制应力的方法可以有效控制量子点的自组织生长过程。

关键词：动力学蒙特卡罗模拟 自组织生长 应力场

Kinetic Monte Carlo Simulation of initial nucleation stage of 2D Ge islands

Deng Ning Xiao Hong Chen Peiyi Li Zhijian

CHINESE JOURNAL OF SEMICONDUCTORS, vol24,2003

Initial nucleation stage of 2D Ge islands during the self-organized growth of Ge islands in Si/Ge mismatch system was studied by

Kinetic Monte Carlo (KMC) simulation. The diffusion barrier was corrected by introducing a strain field induced by adsorbed atoms. The influence of stain and substrate temperature on nucleation sites and size was investigated. The nucleation of 2D islands was determined by strain field and the self-organized growth can be controlled by modulating the stain on the surface.

Keywords: Kinetic Monte Carlo simulation self-organized growth strain field

多层Ge量子点的生长及光学特性研究

邓宁 王吉林 黄文涛 陈培毅 李志坚

半导体学报，vol24(9), 2003

用超高真空化学气相淀积系统在Si(100)衬底上生长了多层Ge量子点。分别用TEM和AFM分析了埋层和最上层量子点的形貌和尺寸，研究了量子点层数和Si隔离层厚度对上层Ge量子点的形状和尺寸分布的影响。观察到样品的低温PL谱线有明显蓝移（87meV），对应于Ge量子点的PL谱线的半高宽度（FWHM）为46meV，说明采用UHV/CVD生长的多层量子点适合量子光电器件的应用。

关键词：超高真空化学气相淀积 多层锗量子点 PL谱

Growth of stacked Ge quantum dots and its optical characteristics

Deng Ning Wang Jilin Huang Wentao Chen Peiyi Li Zhijian

CHINESE JOURNAL OF SEMICONDUCTORS, vol24(9), 2003

Stacked Ge quantum dots was grown on Si(100) by ultra-high vacuum chemical vapor deposition(UHV/CVD). The morphology and size distribution of embedded and upper Ge dots were studied by TEM and AFM respectively. The influences of number of layers and thickness of Si spacer on upper Ge dots were investigated as well. Obvious blue shift (87meV) was observed from PL spectrum under 10K. FWHM of Ge dots NP peak is 46meV which indicates the narrow size distribution of stacked Ge dots grown by UHV/CVD.

PECVD 多晶金刚石平面薄膜场发射特性的研究

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真空电子技术，vol244，2003.

以n-Si为衬底，用PECVD方法淀积了多晶金刚石薄膜。采用以金刚石薄膜为阴极的二极管结构测试了场发射特性，在6V/μm的电场下，场发射电流为5μA。研究了场发射的有效势垒随外加电场的变化，发现在有效势垒随外电场变化的曲线中存在一段平台。从理论上对这种现象进行了研究，分析了电子从Si衬底注入金刚石薄膜的方式，认为有效势垒的平台是由于缺陷能级在金刚石禁带中分布不均匀所致，并由此建立了在注入限制情况下多晶金刚石薄膜的场发射模型。根据模型计算得到有效势垒的理论曲线与实验曲线反映了相同的变化规律。

关键词：多晶金刚石薄膜 等离子体化学气相淀积 场致发射

Study of field emission characteristics of polycrystalline diamond films fabricated by PECVD

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Journal of Wide Bandgap Materials, vol10, 2002.

Polycrystalline diamond films were fabricated on n-Si substrates by PECVD. The field emission characteristics were measured by a diode structure using diamond film as cathode. The emission current was 5μA under 6V/μm(emission area is 4mm2). The effective barrier changes with increasing applied voltage, and there is a step in the curve of barrier vs voltage. The step was analyzed through the electron inject mode from Si to diamond films. The step is considered to be the results of unequal interval distribution of defect energy levels in the forbidden gap, thus an injection-limited field emission model was established. The theoretical curve of effective barrier agrees with that of experiments very well.

Keywords: polycrystalline diamond films PECVD field emission

退火制度对PZT铁电薄膜性能的影响

张宁欣、侯生根、任天令、刘理天，

仪器仪表学报，Vol.24(4): 309-310.

铁电薄膜的性质对于硅基MEMS器件有重要的影响，鉴于此本文尝试通过改善退火工艺以提高PZT薄膜的铁电和压电性质。采用溶胶凝胶法，在Si/SiO2/Ti/Pt衬底上制备了PZT铁电薄膜。实验中，采用一次退火工艺和每层退火工艺制备了两种PZT薄膜，采用XRD对薄膜的晶体结构进行分析，通过C－V和I－V特性的研究发现，每层退火工艺有助于提高PZT薄膜的C-V性质，并降低漏导电流。

关键词：退火制度 PZT 溶胶凝胶 漏导电流

Influence of annealing on properties of PZT ferroelectric thin film

Ningxin Zhang, Shenggen Hou,Tianling Ren, Litian Liu,

Chinese Journal of Scientific Instruments, Vol.24(4): 309-310.

Due to the importance of ferroelectric thin films quality on silicon based MEMS, the attempting on improving the ferroelectric and piezoelectric properties of PZT thin film via modification of annealing processing was carried out in this article. PZT thin film was spin-coated on Si/SiO2/Ti/Pt substrate via sol-gel method. During experiment, two annealing methods, thus one final annealing and one annealing for each layer were adopted. The crystalline structure of thin films were analyzed by X-ray diffraction, and C-V, I-V measurements showed an improved C-V performance and lower leakage current in film prepared with one annealing processing for each layer.

Key Words: Annealing Processing PZT Sol-Gel Leakage Current

Ni81Fe19层厚度对自旋阀巨磁电阻性能的影响

曲炳郡 任天令 刘华瑞 刘理天 库万军 李志坚

仪器仪表学报, Vol.24, No.4, 2003

利用超高真空磁控溅射，制备了一种上钉扎结构标准自旋阀：Ta (6nm) / Ni81Fe19 / Co90Fe10 (1nm) / Cu (1.8nm) / Co90Fe10 (3.5nm) / Ir20Mn80 (8nm) / Ta (6nm)，研究了其中Ni81Fe19层厚度对巨磁电阻变化率(MR)的影响，发现: MR对Ni81Fe19层厚度具有强烈依赖性。当Ni81Fe19层厚度位于2~6nm和7~12nm两个范围时，MR分别维持在较高（约8.34%）和较低（约3.34%）的两个水平，而当Ni81Fe19层厚度从6nm增加到7nm时，MR急剧降低，达5%.由此可见，为了得到高MR，此类自旋阀结构中的Ni81Fe19层厚度不能超过6nm.

Influence of $Ni_{81}Fe_{19}$ soft magnetic layer thickness on the giant magnetoresistance for conventional spin valves

Bing Jun Qu, Tian Ling Ren, Hua Rui Liu, Li Tian Liu, Wan Jun Ku, Zhi Jian Li

Chinese Journal of Scientific Instrument, Vol.24, No.4, 2003

A conventional spin valve with top-pinned structure of Ta (6nm) / Ni81Fe19 / Co90Fe10 (1nm) / Cu (1.8nm) / Co90Fe10 (3.5nm) / Ir20Mn80 (8nm) / Ta(6nm) is prepared using a multi-gun magneto sputtering system with ultra-high-vacuum chambers. Influence of Ni81Fe19 soft magnetic layer thickness on the giant magnetoresistance (GMR) is investigated experimentally. With Ni81Fe19 thickness increased from 6nm to 7nm, the magnetoresistance ratio decreases abruptly from 8.34% to 3.34%, whereas it changes slightly within the thickness ranges from 2 to 6nm and from 7 to 12nm. Thus, in order to obtain a spin valve with high magnetoresistance ratio, the Ni81Fe19 thickness has to be less than 6nm.

用于集成磁传感器的热稳定巨磁电阻自旋阀

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仪器仪表学报, Vol.24, No.4, 2003

本文研制了一种传统结构的上钉扎巨磁电阻自旋阀，其结构为: Ta (6nm) / Ni81Fe19 (4.5nm) / Co90Fe10 (1nm) / Cu (1.8nm) / Co90Fe10 (3.5nm) / Ir20Mn80 (11nm) / Ta (3nm)。该自旋阀磁电阻变化率大(9.15%)，交换场高(约200Oe)，矫顽力低(0.85Oe)，灵敏度高，且具有良好的热稳定性，加之与IC工艺兼容，因而是一种制作集成磁场传感器的理想结构。

A conventional spin valve with thermal stable giant magnetoresistance for integrated magnetic sensors

Bing Jun Qu, Tian Ling Ren, Hua Rui Liu, Li Tian Liu, Wan Jun Ku, Zhi Jian Li

Chinese Journal of Scientific Instrument, Vol.24, No.4, 2003

A conventional spin valve with top-pinned structure of Ta (6nm) / Ni81Fe19 (4.5nm) / Co90Fe10 (1nm) / Cu (1.8nm) / Co90Fe10 (3.5nm) / Ir20Mn80 (11nm) / Ta(3nm) is manufactured by means of a multi-gun magneto sputtering system with ultra-high-vacuum chambers. This spin valve has large magnetoresistance ratio (9.15%), low coercive force (0.85Oe), high exchange field (about 200Oe), high sensitivity and outstanding thermal stability. Besides, the process of spin valve is compatible with IC's. Characters mentioned above make this spin valve be capable of application for integrated magnetic sensors.

以环形振荡器作为敏感单元的加速度传感器

张兆华，岳瑞峰，刘理天.

清华大学学报自然科学版. 2004年第41卷第1期

数字化传感器是当前研究的一个热点。本文提出了一种新的数字加速度传感器，它采用做在硅梁上的MOS环形振荡器作为敏感元件，是由两个环形振荡器和一个混频器组成的频率输出型加速度传感器。该传感器具有准数字输出、灵敏度高、温度系数低以及制作工艺简单等特点，其灵敏度可以达到6.91 kHz/g。本文分析了环形振荡器的频率特性，以及环形振荡器谐振频率和加速度的关系，设计并分析了加速度传感器的电路及物理结构，最后给出了试验结果。这种加速度传感器在军事和民用领域有广阔的应用前景。

Novel accelerometer using ring oscillator as sensitive unit

ZHANG Zhaohua,YUE Ruifeng, LIU Litian

J Tsinghua Univ (Sci & Tech), 41(1) 2004

A novel digital accelerometer using Ring Oscillator and mixer is presented. The sensitive unit of this accelerometer is MOS ring oscillators located on silicon beams. Mixer is used as interior signal processor inorder to improve the output signal characteristic. With a digital frequency output signal, the accelerometer has many perfect characteristics such as high senstivity 6.91 kHz/g, low temperature coefficient and simple fabrication process. The frequency characteristic of MOS ring oscillator and its relationship with acceleration are descriped. The MOS ring ocsillator circuits, mixer circuits and physical structures of this accelerometer are designed. The device was fabricated by standard IC process mixed with MEMS process. The accelerometer will have many applications in the future.

MOS环振式数字加速度传感器

张兆华，岳瑞峰，刘理天.

半导体学报. 2004年第24卷第12期

本文提出了一种新的环振式数字加速度传感器，它采用做在硅梁上的MOS环形振荡器作为敏感元件，两个反方向变化的环振输出信号通过集成在片内的混频器实现频率相减。该传感器具有准数字输出、灵敏度高、温度系数低以及制作工艺简单等特点。本文分析了环形振荡器的频率特性，以及环形振荡器的谐振频率和加速度的关系，分析并设计了加速度传感器的环形振荡器电路、混频器电路、物理结构以及制作工艺，并制作了样品，其灵敏度为6.91 kHz/g。

A novel digital accelerometer using MOS ring oscillators

Zhang Zhaohua, Yue Ruifeng, Liu Litian

CHINESE JOURNAL OF SEMICONDUCTORS, 24(12)2004

A novel digital accelerometer using Ring Oscillators (RO) and mixer is presented. It is different from piezoresistive or capacitive accelerometers that the sensitive unit of this novel accelerometer is MOS ring oscillators located on silicon beams. There are two different ring oscillators in this accelerometer. The output signal was achieved by subtracting the syntonic frequency of one ring oscillator from that of another. The subtraction was realized by a mixer located on the bulk silicon. The accelerometer has many perfect characteristics such as high senstivity, low temperature coefficient and simple fabrication process. The best excellence is that digital signal can be achieved directly from the ouput signal of the RO accelerometer. The frequency character of MOS ring oscillator and its relationship with acceleration are descriped. The circuits, physical structures and fabrication processes of RO accelerometer are designed. The sensitivity of fabricated device is 6.91 kHz/g.

以混频器作为信号处理单元的环振式压力传感器

张兆华，岳瑞峰，刘理天.

电子器件. 2003年第26卷第4期

本文提出了一种新的环振式数字压力传感器，它采用做在硅梁上的MOS环形振荡器作为敏感元件，两个反方向变化的环形振荡器的输出信号通过集成在片内的混频器实现频率相减。该传感器具有准数字输出、灵敏度高、温度系数低以及制作工艺简单等特点。本文分析了环形振荡器的频率特性，以及环形振荡器的谐振频率和压力的关系，分析并设计了压力传感器的环形振荡器电路、混频器电路、物理结构以及制作工艺，并制作了样品，其灵敏度为1.52 kHz/kPa。

A ring oscillator pressure sensor using mixer

Zhang Zhaohua, Yue Ruifeng, Liu Litian

CHINESE JOURNAL OF ELECTRON DEVICES，26(4) 2003

A novel digital pressure sensor using Ring Oscillators (RO) and mixer is presented. The sensitive unit of this pressure sensor is MOS ring oscillators located on silicon films. There are two different ring oscillators in this accelerometer with the same electrical parameters. The output signal was achieved by subtracting the syntonic frequency of one ring oscillator from that of another. The subtraction was realized by a mixer located on the bulk silicon. The frequency character of MOS ring oscillator and its relationship with acceleration are descriped. The circuits, physical structures and fabrication processes of RO accelerometer are designed. The sensitivity of fabricated device is 1.52 kHz/kPa.

混频式环振压力传感器

张兆华，岳瑞峰，刘理天.

仪器仪表学报. 第24卷，第4期（增刊），pp: 210-211，2003年8月

为了解决传感器的数字化，本文提出了一种新的环振式数字压力传感器，它采用做在硅梁上的MOS环形振荡器作为敏感元件，采用混频器作为片内的信号处理单元，实现环形振荡器的频率相减。该传感器的输出量为频率信号，具有准数字输出、灵敏度高、温度系数低以及制作工艺简单等特点。样品的灵敏度为1.52 kHz/kPa。

A ring oscillator pressure sensor using mixer

Zhang Zhaohua Yue Ruifeng Liu Litian

ELECTRONIC INSTRUMENTATION CUSTOMER，24(4)，2003

A novel digital pressure sensor using Ring Oscillators (RO) and mixer is presented. The sensitive unit of this pressure sensor is MOS ring oscillators located on silicon films. There are two different ring oscillators in this accelerometer with the same electrical parameters. The output signal was achieved by subtracting the syntonic frequency of one ring oscillator from that of another. The subtraction was realized by a mixer located on the bulk silicon. The sensitivity of fabricated device is 1.52 kHz/kPa.

MOS环形振荡器在传感器中的应用

张兆华，岳瑞峰，刘理天.

第八届全国敏感元件与传感器学术会议（STC03），北京，2003年11月.

本文提出了一种新的数字加速度传感器，它采用做在硅梁上的MOS环形振荡器作为敏感元件，利用混频器作为片内信号处理单元，该传感器具有准数字输出、灵敏度高、温度系数低以及制作工艺简单等特点。本文分析了环形振荡器的频率特性，以及环形振荡器谐振频率和加速度的关系，分析并设计了加速度传感器的电路及物理结构，最后给出了试验结果。

The application of MOS ring oscillator in sensors

ZHANG Zhaohua,YUE Ruifeng, LIU Litian

A novel digital accelerometer using Ring Oscillator and mixer is presented. The sensitive unit of this accelerometer is MOS ring oscillators located on silicon beams. Mixer is used as interior signal processor inorder to improve the output signal characteristic. With a digital frequency output signal, the accelerometer has many perfect characteristics such as high senstivity, low temperature coefficient and simple fabrication process. The frequency characteristic of MOS ring oscillator and its relationship with acceleration are descriped. The MOS ring ocsillator circuits, mixer circuits and physical structures of this accelerometer are designed. The device was fabricated by standard IC process mixed with MEMS process.

用于硅衬底隔离的选择性多孔硅厚膜的制备

陈忠民，刘泽文，刘理天，李志坚

第六届全国微米纳米会议

在硅衬底上形成高阻隔离层对于提高硅基射频电路的性能具有重要意义。采用多孔硅厚膜作为隔离层，能够极大地降低衬底高频损耗。本文对N+型硅衬底上选择性多孔硅厚膜的制备进行了研究。通过在阳极氧化反应中采用不同的HF溶液的浓度、电流密度和反应时间来控制多孔硅的膜厚、孔隙度等特性。有效地减少了多孔硅的龟裂失效。得到的多孔硅最大膜厚为72μm。测量了多孔硅的生长速率与表面形貌。

Formation of Selective Thick Porous Silicon Layers for Insulating Si Substrate

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Using thick layers of Porous Silicon（PS）as insulating layer can greatly decrease the high frequency loss of Si substrate. In this

paper Porous Silicon formation on N+ substrate is researched. Porous silicon layers of different thickness and porosities are obtained using anodization method via controlling the hydrofluoric acid concentration, current density and time. Cracks of Porous Silicon are effectively diminished. The maximal thickness of PS layers is 72μm. Formation rate of PS and morphology are measured.

用于衬底隔离的选择性氧化多孔硅厚膜的制备

陈忠民 刘泽文 刘理天 李志坚

第六届全国微米纳米会议

本文对N+型硅衬底上用于衬底隔离的选择性氧化多孔硅厚膜的制备进行了研究。实验过程中通过控制阳极氧化反应中HF溶液的浓度、电流密度和反应时间形成了不同厚度和孔隙度的多孔硅厚膜，并采用两步氧化的方法得到氧化多孔硅厚膜。实验得到的平整的氧化多孔硅厚膜最大厚度为60μm。对氧化多孔硅作为衬底隔离材料应用于硅基射频集成电路进行了初步的探索。

关键词：多孔硅 氧化多孔硅 射频

Formation of Selective Thick OPS Layers for Insulating Substrate

Chen Zhongmin Liu Zewen Liu Litian Li Zhijian

Chinese Journal of Scientific Instrument, 2003

Selective thick layers of oxidized porous silicon (OPS) formation on N+ substrate is researched. Porous silicon layers of different thickness and porosities are obtained using anodization method via controlling the hydrofluoric acid concentration, current density and time. The thick porous silicon layers are oxidized by a two-step oxidation method. The maximal thickness of OPS layers is 60μm. Research on OPS as a possible insulating material for radio frequency integrated circuits application is performed.

适用于GMR传感器的高性能自旋阀研究

刘华瑞 任天令 刘理天 库万军

第一届全国信息获取与处理学术会议

在玻璃和硅衬底上利用高真空直流磁控溅射的方法淀积了结构为Ta/NiFe/CoFe/Cu/CoFe/IrMn/Ta的IrMn顶钉扎自旋阀薄膜。分别研究了增加磁电阻率，降低矫顽力和提高交换场的方法。经过结构的改善和工艺条件的优化后，使自旋阀的磁电阻率达到9.12%，矫顽力为1.04×(103/4π)A/m。通过2分钟的RIE使矫顽力减小33%，而磁电阻率几乎不受影响。利用CoFe/Cu/CoFe SAF结构使交换场从180×(103/4π)A/m上升到600×(103/4π)A/m左右。这种高性能的自旋阀适用于具有广泛前景的GMR传感器。

Investigation of high performance spin valve for GMR sensors

Liu Huarui, Ren Tianling, Liu Litian, Ku Wanjun

Chinese Journal of Scientific Instrument, Vol.24, No.4, 2003

IrMn top spin valves, with a structure of Ta/NiFe/CoFe/Cu/CoFe/IrMn/Ta, were deposited on glass and silicon substrate by high vacuum DC magnetron sputtering. The spin valves have a MR of 9.12% and a coercivity of 1.04×(103/4π)A/m after the optimizing of the structure parameters and the fabrication conditions. The exchange bias field was enhanced from 180×(103/4π)A/m to about 600×(103/4π) A/m utilizing SAF structure (CoFe/Cu/CoFe). The coercivity was reduced 33% using a 2 minutes RIE process, which had a negligible effect on the MR.

SOI结构P型SiGe沟道混合模式晶体管器件模型研究

夏克军 李树荣 陈培毅 钱佩信

半导体学报 2 4(3)2 0 0 3年 3月p312-317

在带有应变SiGe沟道的SOI MOSFET结构中，把栅和衬底相连构成了新型的混合模式晶体管 (SiGe SOI BMHMT).在SIVACO软件的器件数值模拟基础上，对这种结构的P型沟道管工作过程作了分析，并建立了数学模型。提出在低电压 (小于 0.7 V)下，衬底电极的作用可近似等效成栅，然后依据电荷增量 (非平衡过剩载流子)的方法，推导出该结构的I-V特性方程。该方程的计算结果与器件模拟结果相一致。

Device Model for SOI P-Type Bipolar-MOS Hybrid Mode Transistors with Strained SiGe Layer

Xia Kejun, Li Shurong, Chen Peiyi, Qian Peixin

Chinese Journal of Semiconductors, 24(3), 2003, p312-317

Based on the structure of SOI MOSFET with a buried strained SiGe layer, a novel bipolar MOS hybrid mode transistor (SiGe SOI BMHMT) is generated by connecting the gate to its substrate. A mathematic model for such a transistor of p type is presented grounding on the numerical device sumulation carried out by the software SIVACO. It is demonstrated that the substrate electrode can be regarded as a

gate under the condition of low voltage supply (<0.7V). The equation of its I-V characteristics is then deduced according to the method of charge increment. The calculated results of this equation are consistent with the ones from the numerical device simulation.

Si Ge沟道 SOI CMOS的设计及模拟

李树荣，王 纯，陈培毅，黎 晨

固体电子学研究与进展, Vol. 2 3, No. 2, p214-218(2 0 03)

在 SOI(Silicon on Insulator)结构硅膜上面生长一层 Si Ge合金，采用类似 SOICMOS工艺制作成具有Si Ge沟道的 SOI CMOS集成电路。该电路不仅具有 SOI CMOS电路的优点，而且因为 Si Ge中的载流子迁移率明显高于 Si中载流子的迁移率，所以提高了电路的速度和驱动能力。另外由于两种极性的 SOI MOSFET都采用 Si Ge沟道，就避免了只有 SOIPMOSFET采用 Si Ge沟道带来的选择性生长 Si Ge层的麻烦。采用二维工艺模拟得到了器件的结构，并以此结构参数进行了器件模拟。模拟结果表明，