# 一种用于表征亚阈值电流镜电路中CMOS工艺波动的统计学方法

## A Statistical Method for Characterizing CMOS Process Fluctuations in Subthreshold Current Mirrors

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中文摘要：

　　提出了一种新的表征亚阈值电路镜电路中CMOS工艺波动的方法. 与现有的统计学方法相比，该方法在理论上和计算复杂度上相对简洁，但对亚阈值电流镜电路中的CMOS工艺波动做出了准确的评估. 此模型利用统计学的概念将依赖于IC工艺的物理参数抽象为具有确定均值和方差的随机变量，并进一步将所有随机因素累加为离散鞅. 在SMIC 0.18μm CMOS 1P6M 混合信号工艺下，利用工作在100pA~1μA范围内、增益为100的亚阈值电流镜电路对此方法的正确性进行了实验验证. 该理论成功地预测了~ 10%的实测芯片间工艺波动，并且给出了~1mV的片上阈值电压标准偏差，此结果与SMIC提供的设计参数吻合. 该理论给出的概率分布与实测结果的偏差小于8%. 同时，还针对高工艺稳定性的亚阈值模拟电路设计方法进行了相关的讨论.

英文摘要：

　　A novel method to characterize CMOS process fluctuations in subthreshold current mirrors (SCM) is reported. The proposed model is succinct in methodology and calculation complexity compared with previous statistical models. However, it provides favorable estimations of CMOS process fluctuations on the SCM circuit, which makes it promising for engineering applications. The model statistically Abstracts physical parameters, which depend on the IC process, into random variables with certain mean values and standard deviations, while aggregating all the random impacts into a discrete martingale. The correctness of the proposed method is experimentally verified on an SCM circuit implemented in an SMIC 0.18μm CMOS 1P6M mixed signal process with a conversion factor of 100 in an input range from 100pA to 1μA. The proposed theory successfully predicts ~10% of die-to-die fluctuation measured in the experiment, and also suggests the ~1mV of threshold voltage standard deviation over a single die, which meets the process parameters suggested by the design kit from the foundry. The deviations between calculated probabilities and measured data are less than 8%. Meanwhile, pertinent suggestions concerning high fluctuation tolerance subthreshold analog circuit design are also made and discussed.