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论文

绝热无比型动态触发器和同步时序电路综合

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摘要
该文从电路三要素理论出发研究低功耗电路,定量描述绝热无比型动态记忆电路。绝热无比型动态触发器利用电容接收和保存信息,避免目前绝热电路中电容上的信息得而复失的现象,其中绝热D和T’触发器只用6管,带‘与或非’输入的绝热D触发器只用9管。在上述理论基础上该文提出绝热无比型动态同步时序电路综合方法,用此法设计出绝热5421BCD码十进制计数器,仅用32管,总功耗小于一个PAL-2N四位二进制计数器的功耗,计算机模拟验证该文方法正确。

关键词 绝热无比型动态触发器 绝热同步时序电路综合 电路三要素理论

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Adiabatic ratioless dynamic flip-flops and synthesis for synchronos sequential circuits

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Abstract
In this paper a synthesis for low power circuits is studied and an adiabatic ratioiess dynamic memory circuit is expressed quantitatively in accordance with the theory of three essential circuit elements. Then many adiabatic ratioiess dynamic flip-flops are composed of two adiabatic ratioiess dynamic latches, for example D or T’ flip-flop of 6 MOS transistors and D flip-flop with AND-NOR-inputs of 9 MOS transistors, in which there is no phenomenon of information disappearing rapidly after receiving one in capacitors. On the basis of above theory, this paper presents a synthesis for adiabatic synchronous sequential circuits, and designs an adiabatic 5421BCD decimal counter circuit of 32 MOS transistors which consumes lower power than that of an adiabatic PAL-2N 4-bit binary counter. Above theory is vertified by computer simulation.

Key words Adiabatic ratioless dynamic flip-flops Synthesis for adiabatic synchronous sequential circuits Theory of three essential circuit elements

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