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Effect of Clock and Power Gating on Power Distribution Network Noise in 2D and 3D Integrated Circuits

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Abstract
In this work, power supply noise contribution, at a particular node on the power grid, from clock/power gated blocks is maximized at particular time and the *synthetic* gating patterns of the blocks that result in the maximum noise is obtained for the interval 0 to target time. We utilize wavelet based analysis as wavelets are a natural way of characterizing the time-frequency behavior of the power grid. The gating patterns for the blocks and the maximum supply noise at the Point of Interest at the specified target time obtained via a Linear Programming (LP) formulation (clock gating) and Genetic Algorithm based problem formulation (Power Gating).

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