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国家重点基础研究

基于FPGA与ARM的智能合并单元设计

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摘要:

针对智能变电站信息数字化、功能集成化、结构紧凑化的要求, 分析了IEC 60044-8、IEC 61850-9-1/2标准对合并单元的定义, 在此基础上设计了一种基于现场可编程门阵列(field-programmable gate array, FPGA)与高级RISC微处理器(advanced RISC machines, ARM)的智能合并单元。辅处理器FPGA负责多路数据的同步接收, 并集成逻辑判别机制软件实现母线的并列运行和切换; 主处理器ARM负责FPGA的实时控制并将采样值按IEC 61850-9-2标准通过以太网发送, 采用预配置采样值控制块实现采样值传输模型的灵活定义, 避免了制造报文规范(manufacturing message specification, MMS)映射的实现困难。试验结果表明了设计方法的可行性和正确性。

关键词: 智能变电站 合并单元 IEC 61850-9-2 现场可编程门阵列 高级RISC微处理器 信号处理

Design of Smart Merging Unit Based on FPGA and ARM

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Abstract:

To meet the requirements of smart substations for digital information, integrated functions and compact structure, the definitions of merging unit in IEC 60044-8 and IEC 61850-9-1/2 are analyzed, and on this basis a smart merging unit based on field-programmable gate array (FPGA) and advanced RISC machines (ARM) is designed. The auxiliary processor FPGA is responsible for synchronously receiving multi-channel data from different electronic transformers and implementing the parallel operation and switching-over of busbar by integrated logical control mechanism software; the main ARM processor is responsible for the real-time control of FPGA and sending the sampled data in the form specified in IEC 61850-9-2 by Ethernet, and the pre-configured sampled value control block is utilized to implement the flexible definition of transmission model for sampled values to avoid the difficulty in implementing the mapping of manufacturing message specification (MMS). Testing results show that the proposed design is feasible and correct.

Keywords: smart substation merging unit IEC 61850-9-2 field-programmable gate array (FPGA) advanced RISC machines (ARM) signal processing

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