

Sigma-Delta微加速度计非理想因素建模与系统级设计

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摘要:

为了简化Sigma-Delta($\Sigma\Delta$)微加速度计接口电路晶体管级的仿真和优化, 建立了系统中的非理想因素模型, 并在此基础上完成了一种单环结构的 $\Sigma\Delta$ 微加速度计的系统级设计。分析了敏感结构中固定极板运动、时钟抖动、开关热噪声、运算放大器噪声等非理想因素对系统的影响, 并分别建立了Simulink模型。基于所建模型, 设计了一种 $\Sigma\Delta$ 微加速度计的精确的Simulink模型。系统级仿真结果表明: 二阶系统的信号-噪声-谐波失真比(SNDR)为70.1dB, 有效位(ENOB)为11.36位, 四阶系统的SNDR为92.7dB, ENOB为15.7位。相比于晶体管级仿真结果, 基于本文所建立的非理想因素模型的系统仿真可以准确地表述出系统性能, 同时大大缩短了仿真时间, 简化了传感器设计中的参数优化过程。

关键词: 微加速度计; Sigma-Delta; 系统级建模; 非理想因素

Model building of nonideal factors in Sigma-Delta accelerometer and system level design

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Abstract:

Precise models of nonideal factors in capacitive Sigma-Delta ($\Sigma\Delta$) micromachined accelerometer and a Simulink model of single-loop Sigma-delta accelerometer are presented to facilitate the transistor-level simulations and optimization. The influences of main nonideal factors including the motion of fixed electrode, clock jitter, thermal noise of switches and noise of operational amplifier to the system are analyzed. For each nonideal factor, a description of the considered effect as well as the implementation details with Simulink is provided. Based on these models, a precise Simulink model of $\Sigma\Delta$ accelerometer is proposed. The system level simulation results indicate that signal-to-noise-and-distortion ratio (SNDR) of second-order system is 70.1dB, effective number of bits (ENOB) is 11.36bits, and SNDR of fourth-order system is 92.7dB, ENOB is 15.7bits. Compared with transistor-level simulations, the system model could describe the performance of system accurately, meanwhile saving the simulation time and simplifying the process of optimization greatly.

Keywords: Micromachined accelerometer; Sigma-Delta; Nonideal factor; System level

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