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器件驱动与控制

# FPGA配置过程监控系统设计

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摘要： 为了解决系统上电后FPGA应用程序配置失败的问题,设计了FPGA配置过程监控系统。深入分析了FPGA配置的工作流程,阐述了FPGA配置监控系统的核心监控电路、监控软件的设计思想、代码实现及仿真验证过程。最后,用MATLAB对实验数据进行分析处理,得出了FPGA器件的配置失败率和失败曲线以验证设计的可行性和优越性。实验结果表明:利用该系统可以使FPGA配置成功率达到100%,比传统设计方法的FPGA配置成功率提高了0.041%,满足了系统对FPGA配置应用程序成功率高、可靠性强的要求。应用结果显示,FPGA配置监控系统能及时监测出FPGA配置过程所出现的异常,判断分析出问题的根源,最终使FPGA应用程序在系统一次性上电后配置成功。

关键词： FPGA配置 监控状态机 看门狗计时器 虚拟模型 MATLAB

# Design of FPGA Configuration Monitoring System

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Abstract: In order to solve the problem of FPGA configuration failure when the satellite camera is power-on, a FPGA configuration process monitoring system was designed. First, the process and principle of FPGA configuration were analyzed in detail. Then, this paper described the core monitoring circuit in the FPGA configuration monitoring system, the design ideas of software for the monitoring system, code implementation and simulation procedures for monitoring FPGA configuration. Finally, the experiment data were processed by MATLAB software, and thus FPGA device configuration failure rate and failure rate curve were obtained to verify the feasibility and superiority of the design. Experiment results indicate that by using the system the success rate of FPGA configuration is up to 100%. Compared with the traditional methods of FPGA configuration, the new design made configuration success rate increased by 0.041%,can satisfy the satellite camera s requirements of high success rate and reliability of configuring the FPGA application. This scheme has been applied to the development of a certain space camera. The application results show that the FPGA configuration monitoring system can monitor timely exception which occurs in the process of FPGA configuration and can analyze the error origins and can configure successfully the FPGA applications when the satellite camera is one-time power-on.

Keywords: FPGA configuration monitor state machine watchdog timer virtual model MATLAB

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