

CMOS图像传感器中分段电容DAC非理想因素研究

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基金项目：国家自然科学基金

摘要：

CMOS图像传感器信号处理中通常采用分段电容DAC产生斜坡参考电压。研究了分段电容DAC精确的电容失配及寄生与其转换精度的关系式。基于对分段电容DAC工作原理的研究，导出了电容失配及寄生模型；针对其分数桥接电容失配、各二进制电容间的失配及寄生电容问题进行了理论分析；采用Spectre软件对分段电容DAC进行非理想因素仿真，设计了一个采用分段电容DAC的10位单斜ADC并对其进行测试，仿真和测试结果均验证了理论分析的正确性。上述理论分析结果可作为分段电容DAC的设计指导。

关键词：微电子学与固体电子学；分段电容DAC；电容失配；寄生；转换精度

Research on Non-Ideal Factors of Segmented-Capacitor DAC in CMOS Image Sensor

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Abstract:

segmented-capacitor digital analog converter (SC DAC) is usually used in CMOS image sensor to generate a ramp reference voltage. Precise relationships between conversion resolution and non-ideal factors segmented-capacitor digital analog converter are derived. These non-ideal factors consist of coupling capacitor mismatch, binary-weighted-capacitor mismatch and parasitic effects. Initially, based on the study of SC DAC operation principle, mathematical models are established. Then the effects of non-ideal factors on SC DAC are analyzed. Simulation and measurement results verify the theoretical analysis. These precise relationships serve as a guideline for the design of SC DAC.

Keywords: microelectronics and solid electronics; segmented-capacitor DAC; capacitor mismatch; parasitic; conversion resolution

投稿时间：2013-12-01

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