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一种基于电平位移电路的低电压全摆幅CMOS运放

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摘 要：为解决阈值电压对电源电压和输入信号的受限问题，提出一种实用的电平位移电路，为运放的输入级提供良好的电平位移。采用互补金属氧化物半导体(CMOS) 0.5 μm工艺设计的低电压全摆幅CMOS 运算放大器，中间级采用适合低电压工作的低压宽摆幅共源共栅结构，输出级采用传统的Class A类得到轨至轨的输出。采用Hspice软件对所设计的电路进行仿真。研究结果表明：当电源电压降至或者小于NMOS与PMOS的阈值电压之和时，在任何共模输入电压下，该运放都能正常工作，实现输入级的全摆幅和恒跨导；在1.3 V单电源供电情形下直流开环增益达106.5 dB，单位增益带宽为2.3 MHz，功耗178.8 μW。电路结构简单紧凑，具有实用的电平位移功能，适合于低电压应用。

关键字：CMOS运放；全摆幅；仿真；电平位移技术

A level-shifting circuit based on low-voltage rail-to-rail CMOS op-amp

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Abstract:A level-shifting circuit was proposed to solve the supply voltage and input signal limited by threshold voltage, which offers a level-shifting voltage for input stage. A low-voltage rail-to-rail op-amp was designed by CMOS 0.5 μm, the middle gain stage uses the low voltage, wide swing cascade structure which is suitable to work in low voltage, and the output stage uses the traditional class A to reach rail-to-rail. With a single 1.3 V supply voltage, the whole circuit was simulated in Hspice. The results show that when the supply voltage is equal to or lower than the sum of NMOS threshold voltage and PMOS threshold voltage, the op-amp can also work well in any common mode input voltage. It reaches rail-to-rail common mode input range and constant g_m. The direct current gain is 106.5 dB while the unit gain bandwidth is 2.3 MHz, and 178.8 μW power dissipation. For its simple and compact structure, this op-amp cell is suitable for low voltage application.

Key words:CMOS op-amp; rail-to-rail; simulation; level-shifting technique

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