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San Jose Convention Center
San Jose, California, United States
24 - 28 February 2019

Design-Process-Technology Co-optimization for Manufacturability XIII

Wednesday - Thursday 27 - 28 February 2019

Conference Sessions At A Glance

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Important Dates

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Abstract Due:
29 August 2018

Manuscript Due Date:
19 January 2019

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WEDNESDAY 27 FEBRUARY

Show All Abstracts

Session 1: Design-Technology Co-optimization

Wednesday 27 February 2019
8:00 AM - 10:00 AM

Session Chairs: Jason P. Cain, Advanced Micro Devices, Inc. (United States) ; Chi-Min Yuan, NXP Semiconductors (United States)

Standard-cell design architecture options below 5nm node: The ultimate scaling of FinFET and Nanosheet *(Invited Paper)*
Paper 10962-1
Author(s): Syed Muhammad Yasser Sherazi, Miroslav Cupak, Peter Debacker, Diederik Verkest, Anda C. Mocuta, Ryoung-Han R. Kim, Alessio Spessot, Julien Ryckaert, IMEC (Belgium)

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Optimization of read and write performance of SRAMs for node 5nm and beyond
Paper 10962-2
Author(s): Khaja Ahmad Shaik, Mohit Gupta, Pieter Weckx, Alessio Spessot, IMEC (Belgium)

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A novel design-for-yield solution based on interconnect level layout improvements at 7nm technology node
Paper 10962-3
Author(s): Jaehwan Kim, Sangah Lee, Byungchul Shin, Junsu Jeon, Jin Kim, Byung-Moo Kim, Jae-Hyun Kang, Seung Weon Paek, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Piyush Pathak, Frank E. Gennari, Philippe Hurat, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States)

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Backside power delivery as a scaling knob for future systems
Paper 10962-4
Author(s): Bharani Chava, Khaja Ahmad Shaik, Anne Jourdain, Peter Debacker, IMEC (Belgium); Sofiane Guissi, Coventor, SARL (France); Julien Ryckaert, Geert Van Der Plaas, Alessio Spessot, Eric Beyne, Anda C. Mocuta, Diederik Verkest, IMEC (Belgium)
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CFET Standard-cell design down to 3Track height for node 3nm and below
Paper 10962-5
Author(s): Syed Muhammad Yasser Sherazi, Alessio Spessot, Julien Ryckaert, Ryoung-Han R. Kim, IMEC (Belgium)
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Session 2: Layout Analytics

Wednesday 27 February 2019
10:30 AM - 12:10 PM

Session Chairs: Lars W. Liebmann, GLOBALFOUNDRIES Inc. (United States) ; Ru-Gun Liu, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

Persistent homology analysis of complex high-dimensional layout configurations for IC physical designs
Paper 10962-6
Author(s): Yacoub Kureh, Univ. of California, Los Angeles (United States), Motivo, Inc. (United States); Vito Dai, Luigi Capodieci, Motivo, Inc. (United States)
Add To My Schedule

Machine learning based wafer defect detection and repair
Paper 10962-7
Author(s): Yuansheng Ma, Mentor, a Siemens Business (United States)
Add To My Schedule

Pattern-aware diagnostics: using high-performance pattern analysis to identify defect root cause
Paper 10962-8
Author(s): Jason P. Cain, Abdullah Yassine, Moutaz Fakhry, Advanced Micro Devices, Inc. (United States); Piyush Pathak, Jeffrey E. Nelson, Frank E. Gennari, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States)
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Fast detection of largest repeating layout pattern
Paper 10962-9
Author(s): Jingsong Chen, The Chinese University of Hong Kong (Hong Kong, China); James Shiely, Synopsys Inc. (United States)
Add To My Schedule

Process window-based feature and die failure rate prediction
Paper 10962-10
Author(s): John L. Sturtevant, Lianghong Yin, Young Chang Kim, Shumay Shang, Andrew Burbine, Sara Khalaf, Germain Fenger, Mentor Graphics Corp. (United States)
Add To My Schedule

Lunch/Exhibition Break 12:10 PM - 1:40 PM

Session 3: Machine Learning

Wednesday 27 February 2019
1:40 PM - 3:20 PM

Session Chairs: Luigi Capodieci, Motivo, Inc. (United States) ; Lynn T. N. Wang, GLOBALFOUNDRIES Inc. (United States)

Applications of machine learning in EDA *(Invited Paper)*
Paper 10962-11
Author(s): Paul D. Franzon, North Carolina State Univ. (United States)
Add To My Schedule

Optical proximity correction using bidirectional recurrent neural network (BRNN)
Paper 10962-12
Author(s): Yonghwi Kwon, KAIST (Korea, Republic of); Youngsoo Song, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Youngsoo Shin, KAIST (Korea, Republic of)
Add To My Schedule

Investigation of machine learning for dual OPC and assist feature printing optimization
Paper 10962-13
Author(s): Kevin Hooker, Marco Guajardo, Synopsys, Inc. (United States); Rich Wu, Synopsys Taiwan Co., Ltd. (Taiwan); Peter Brooker, Kevin Lucas, Synopsys, Inc. (United States)
Add To My Schedule

Using machine learning in the physical modeling of lithographic processes
Paper 10962-14
Author(s): Kostas Adam, Shashidhara K. Ganjugunte, Mentor, a Siemens Business (United States); Clement Moyroud, Mentor Graphics (Ireland) Ltd. French Branch (France); Kanstantsin Shchehlik, Michael C. Lam, Andrew Burbine, Germain L. Fenger, Mentor, a Siemens Business (United States)
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Session 4:
Process Modeling and Layout Optimization

Wednesday 27 February 2019
3:50 PM - 5:30 PM

Session Chairs: Neal V. Lafferty, Mentor, a Siemens Business (United States) ; Shigeki Nojima, Toshiba Corp. (Japan)

Design for manufacturability for analog, radio frequency, and millimeter wave designs
Paper 10962-15
Author(s): Lynn T. N. Wang, Gail Katzman, GLOBALFOUNDRIES Inc. (United States); Yongfu Li, GLOBALFOUNDRIES Singapore Pte. Ltd. (United States); Vikas Mehrotra, Janam Bakshi, Ahmed Abdulghany, Michael Simcoe, Rais Huda, Vijay Kanagala, Don Blackwell, GLOBALFOUNDRIES Inc. (United States); Thomas Hermann, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG (United States); Uwe Paul Schroeder, Thomas McKay, Sriram Madhavan, GLOBALFOUNDRIES Inc. (United States)
Add To My Schedule

3D resist reflow compact model for imagers microlens shape optimization
Paper 10962-16
Author(s): Sébastien Bérard-Bergery, Jérôme Hazart, Patrick Quéméré, Jean-Baptiste Henry, CEA-LETI (France); Charlotte Beylier, STMicroelectronics S.A. (France); Nacima Allouti, Maryline Cordeau, Raphaël Eleouet, Florian Tomaso, CEA-LETI (France); Valérie Rousset, Alain Ostrovsky, STMicroelectronics S.A. (France)
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Accuracy improvement of electrical characteristics estimation for sub-20nm FDSOI devices with non-rectangular gates
Paper 10962-17
Author(s): Jia-Syun Cai, Chien-Lin Lee, Sheng-Wei Chien, Kuen-Yu Tsai, National Taiwan Univ. (Taiwan)
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Optimizing DFM scores by using a genetic evolution algorithm
Paper 10962-18
Author(s): Uwe Paul Schroeder, GLOBALFOUNDRIES Inc. (United States)
Add To My Schedule

Full-chip layout optimization for photo process window improvement of 3D NAND metal routing level
Paper 10962-19
Author(s): Jennefir L. Digaum, Hung-Eil Kim, Eric L. Christensen, Hamilton Sanchez, Moydul Islam, Micron Technology, Inc. (United States)
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Session PS1:
Posters-Wednesday

Wednesday 27 February 2019
5:30 PM - 7:30 PM

Posters will be on display from 10:00 am to 5:00 pm, and again from 5:30 pm to 7:30 pm during the poster session. Come to view the high-quality papers that are presented in this alternative format, and interact with the poster authors who will be present during the poster session. Enjoy light refreshments while networking with your colleagues.

Full author or technical registration is required for entry to the poster session. Please wear your registration badge.

SALELE process from theory to fabrication
Paper 10962-30
Author(s): Youssef Drissi, IMEC (Belgium); Ahmed Hamed Fatehy, Rehab K. Ali, Mentor Graphics Egypt (Egypt); Germain Fenger, Mentor, a Siemens Business (United States); Werner Gillijns, IMEC (Belgium); James Word, Mentor, a Siemens Business (United States)
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Pareto exploration of STT-MRAM footprint as a last-level caches in high-performance computing domain
Paper 10962-31
Author(s): Khaja Ahmad Shaik, IMEC (Belgium)
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Sample patterns extraction from layout automatically based on hierarchical cluster algorithm for lithography process optimization
Paper 10962-32
Author(s): Tianyang Gai, Ying Chen, Pengzheng Gao, Xiaojing Su, Institute of Microelectronics (China), Univ. of Chinese Academy of Sciences (China); Lisong Dong, Institute of Microelectronics (China); Yayi Wei, Institute of Microelectronics (China), Univ. of Chinese Academy of Sciences (China); Yajuan Su, Institute of Microelectronics (China); Tianchun Ye, Institute of Microelectronics (China), Univ. of Chinese Academy of Sciences (China)
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Incorporating process variation contours in design rule calculation and SRAM design optimization
Paper 10962-33
Author(s): Dongbing Shao, IBM Corp. (United States)
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Practical lithography hotspot identification using mask process model
Paper 10962-34
Author(s): Yohan Choi, Photronics, Inc. (United States); Pai Chi Chen, Chain Ting Huang, Shang Feng Weng, Cloud Cheng, United Microelectronics Corp. (Taiwan); Colbert Lu, Photronics DNP Semiconductor Mask Corp. (Taiwan); Young Ham, Michael Green, Mohamed Ramadan, Photronics, Inc. (United States); Hong Jen Lee, Photronics DNP Semiconductor Mask Corp. (Taiwan); Chris Progler, Photronics, Inc. (United States)
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Copper interconnect topography simulation method in 3D NAND design for manufacturing flow
Paper 10962-35
Author(s): Bifeng Li, Yang Li, Jinxin Li, Peng Jiang, Yangtze Memory Technologies Co., Ltd. (China); Zhengfang Liu, Chunshan Du, Mentor Graphics Shanghai Electronic Technology Co. (China); Ruben Ghulghazaryan, Mentor Graphics Corp. (Armenia); Qijian Wan, Xinyi Hu, Mentor Graphics Shanghai Electronic Technology Co. (China)
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FEOL CMP modeling challenge and solution in 3D NAND
Paper 10962-36
Author(s): Bifeng Li, Yang Li, Jinxin Li, Peng Jiang, Yangtze Memory Technologies Co., Ltd. (China); Zhengfang Liu, Mentor Graphics Shanghai Electronic Technology Co. (China); Chunshan Du, Yangtze Memory Technologies Co., Ltd. (China); Ruben Ghulghazaryan, Mentor Graphics Corp. (Armenia); Qijian Wan, Xinyi Hu, Mentor Graphics Shanghai Electronic Technology Co. (China)
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Design rule exploration for width sensitive zone for metal layers in advanced nodes
Paper 10962-37
Author(s): Xiaojing Su, Lisong Dong, Yayi Wei, Yajuan Su, Institute of Microelectronics (China); Chunshan Du, Mentor Graphics Shanghai Electronic Technology Co. (China)
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Experimental study of the strong halation-effect of a fully PGMEA-based under-layer on a highly etched topography in the dual Damascene via-first approach
Paper 10962-38
Author(s): Valentina Dall'Asta, STMicroelectronics SRL (Italy)
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An efficient way of automatic layout decomposition and pattern classification
Paper 10962-39
Author(s): Qijian Wan, Xinyi Hu, Zhengfang Liu, Chunshan Du, Mentor Graphics Corp. (China)
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A smart approach for fast lithography hotspots detection
Paper 10962-40
Author(s): Xinyi Hu, Qijian Wan, Zhengfang Liu, Chunshan Du, Mentor Graphics Corp. (China)
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Machine learning to improve accuracy of fast lithographic hotspot detection
Paper 10962-41
Author(s): Namjae Kim, KiHeung Park, Jiwon Oh, Sangwoo Jung, Sangah Lee, Jae-Hyun Kang, Seung Weon Paek, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Kareem Madkour, Mentor Graphics Egypt (Egypt); Wael ElManhawy, Mentor Graphics Corp. (United States); Aliaa Kabeel, Ahmed ElGhoroury, Marwah Shafee, Asmaa Rabie, Mentor Graphics Egypt (Egypt); Joe Kwan, Mentor Graphics Corp. (United States)
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THURSDAY 28 FEBRUARY Show All Abstracts

Session 5: Design Interactions with Metrology: Joint session with conferences 10959 and 10962

Thursday 28 February 2019
8:00 AM - 10:00 AM

Session Chairs: John A. Allgair, BRIDG (United States) ; Ryoung-Han R. Kim, IMEC (Belgium)

AI: from deep learning to in-memory computing *(Keynote Presentation)*
Paper 10959-53
Author(s): Hsiang-Lan Lung, Macronix (United States)
Add To My Schedule

Critical defect detection, monitoring and fix through process integration engineering by using D2DB pattern monitor solution
Paper 10962-20
Author(s): Abhishek Vikram, Anchor Semiconductor, Inc. (United States); Ming Tian, Yu Zhang, Tiapeng Guan, Jianghua Leng, Baojun Zhao, Lei Yan, Wei Hua, Shanghai Huali Microelectronics Corp. (China); Shijie Chen, Guojie Chen, Hui Wang, Gary Zhang, Wenkui Liao, Anchor Semiconductor, Inc. (China)
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Massive metrology and failure identification for DRAM applications
Paper 10959-54
Author(s): Harm Dillen, Dorothe Oorschot, Marleen Kooiman, Willem van Mierlo, Ziyang Wang, ASML Netherlands B.V. (Netherlands); Kang-San Lee, Jin-Woo Lee, ASML Korea Co., Ltd. (Korea, Republic of); Ruochong Fei, Shu-Yu Lai, Marc Kea, Hermes-Microvision Inc., USA (United States); Inhwan Lee, Hwan Kim, Junghyun Kang, Jaehee Hwang, Chang-Moon Lim, SK Hynix, Inc. (Korea, Republic of)
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Mark sensitivity of uDBO and IBO in advanced DRAM node
Paper 10962-21
Author(s): Chun-Wei Chen, ASML Taiwan Ltd. (Taiwan)
Add To My Schedule

3D optical proximity model optimization using inline 3DSEM metrology
Paper 10959-55
Author(s): Shimon Levi, Applied Materials Israel, Ltd. (Israel); Hans-Jurgen Stock, Wolfgang Demmerle, Synopsys GmbH (Germany)
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Session 6:
EUV OPC and Modeling: Joint session with conferences 10957 and 10962

Thursday 28 February 2019
10:30 AM - 12:10 PM

Session Chairs: Kevin Lucas, Synopsys, Inc. (United States) ; Soichi Inoue, Toshiba Corp. (Japan)

Development of fast rigorous simulators for large-area EUV lithography simulation
Paper 10957-45
Author(s): Michael Yeung, Fastlitho Inc. (United States); Eytan Barouch, Boston Univ. (United States)
Add To My Schedule

Mask 3D effect reduction and defect printability of etched multilayer EUV mask
Paper 10957-46
Author(s): Takashi Kamo, Takeshi Yamane, Yasutaka Morikawa, Susumu Iida, Takayuki Uchiyama, Shunko Magoshi, Satoshi Tanaka, Evolving Nano-process Infrastructure Development Ctr., Inc. (Japan)
Add To My Schedule

SAQP spacer merge and EUV self-aligned block decomposition at 28nm metal pitch on imec 7nm node
Paper 10962-22
Author(s): Jae Uk Lee, Syed Muhammad Yasser Sherazi, IMEC (Belgium); Soo-Han Choi, Synopsys, Inc. (United States); Ryoung-Han R. Kim, IMEC (Belgium)
Add To My Schedule

EUV computational lithography using accelerated topographic mask simulation
Paper 10962-23
Author(s): Vitaly Domnenko, Synopsys SPb, LLC (Russian Federation); Bernd Küchler, Wolfgang Hoppe, Jürgen Preuninger, Ulrich Klostermann, Wolfgang Demmerle, Martin Bohn, Dietmar Krüger, Synopsys GmbH (Germany); Ryoung-Han R. Kim, Ling Ee Tan, IMEC (Belgium)
Add To My Schedule

EUV mask synthesis with rigorous ILT for process window improvement
Paper 10962-24
Author(s): Kyle Braam, Guangming Xiao, Synopsys, Inc. (United States); Wolfgang Hoppe, Ulrich Klostermann, Synopsys GmbH (Germany); Kevin Lucas, Synopsys, Inc. (United States)
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Lunch Break 12:10 PM - 1:30 PM

Session 7:
Hotspot Detection

Thursday 28 February 2019
1:30 PM - 3:30 PM

Session Chairs: Vivek K. Singh, Intel Corp. (United States) ; Piyush Pathak, Cadence Design Systems, Inc. (United States)

Lithography hotspot candidate detection using coherence map *(Invited Paper)*
Paper 10962-25
Author(s): Tetsuaki Matsunawa, Taiki Kimura, Shigeki Nojima, Toshiba Memory Corp. (Japan)
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CAPP: context analyzer and printability predictor
Paper 10962-26
Author(s): Vikas Tripathi, Yongfu Li, I-Lun Tseng, Valerio Perez, Zhao Chuan Lee, Jonathan Ong, GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore)
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Hotspot detection using squish-net
Paper 10962-27
Author(s): Haoyu Yang, Piyush Pathak, Frank E. Gennari, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States); Bei Yu, The Chinese Univ. of Hong Kong (Hong Kong, China)
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Multi-criteria hotspot detection using pattern classification
Paper 10962-28
Author(s): Kazufumi Shiozawa, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Toshiya Kotani, Toshiba Memory Corp. (Japan)
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Multilayer CMP hotspot modeling through deep learning
Paper 10962-29
Author(s): Luis Francisco, North Carolina State Univ. (United States); Rui Mao, GLOBALFOUNDRIES Inc. (United States); Ushasree Katakamsetty, GLOBALFOUNDRIES Singapore Pte. Ltd. (Singapore); Piyush Verma, Robert C. Pack, GLOBALFOUNDRIES Inc. (United States)
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